Wei Song (宋威), PhD, Associate Professor

CONTACT INFORMATION

Institute of Information Engineering (IIE)
Chinese Academy of Sciences (CAS)
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Beijing 100085 P.R.China

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ACADEMIC EXPERIENCE

Institute of Information Engineering, CAS, Beijing, P.R.China

November 2017 to present
Associate Professor (11/2017), *supervisor*: Master (09/2018), PhD (09/2019)
Receiver of *CAS pioneer hundred talents*

- Enhance system security with new processor and cache micro-architectures. **(11/2017 — present)**
  - Defense control flow hijacking with hardware managed tagged memory [12,13].
  - Avoid cache side-channel attacks with new cache architectures [8,10,11].
  - Automatic detection of hardware features and parameters [4].
  - Evluating the vulnerabilities of a hardware system using a systematic test suite [3,6,14].
- Open hardware designs for computer architecture research. **(10/2018 — present)**
  - A fast cache model for cache side-channel attack/defense researches [11].
  - Improving the usefulness of open sourced processors [7].

University of Cambridge, Cambridge, UK

November 2014 to October 2017
Research Associate, Computer Laboratory

- LowRISC: An open-source SoC hardware platform using the 64-bit RISC-V ISA. **(11/2014 — 10/2017)**
  - Added tagged memory support to Rocket SoC (L1 D$, L2 and tag cache).
  - Added memory mapped IO support to Rocket core.
  - Untethered Rocket chip SoC.
  - Booted a RISC-V Linux on the untethered Rocket chip using KC705 and Nexys4-DDR boards.
- Large-scale sorter on FPGA for database applications. **(9/2013 — 10/2016)**
  - Parallel merge-sorters to break the speed limit of sequential sorters [16].

The University of Manchester, Manchester, UK

October 2011 to October 2014
Research Associate, School of Computer Science

- EPSRC Project EP/L000563/1: Continuous on-line adaptation in many-core systems: From graceful degradation to graceful amelioration. **(9/2014 — 10/2014)**
  - Investigate the intra/inter-chip task (neuron) migration in the SpiNNaker many-core system.
- EPSRC Project EP/I038306/1: Globally asynchronous elastic logic synthesis. **(10/2011 — 9/2014)**
  - Implemented a RTL Verilog HDL parser using Bison and Flex.
  - Automatic finite state machine (FSM) detection using register relation graphs [23].
  - Automatic data-path extraction using signal-level data flow graphs [22].
  - Automatic interface type recognition.
  - cppRange: A multi-dimensional range calculation library.
- Fault-tolerance techniques for asynchronous on-chip networks. **(9/2012 — 9/2014)**
  - Redundent code for QDI 1-of-N pipeline to avoid errors caused by 1-bit transient fault [5, 9,18,24].
  - Detect and recover from the deadlock caused by permanent faults in asynchronous SDM routers [5,15,17,20,21].

September 2007 to September 2011
Ph.D. in Computer Science, School of Computer Science

- Supervisor: Dr. Doug Edwards

- EPSRC Project EP/E06065X/1: Energy efficient networks-on-chip for dynamically reconfigurable computing platforms.**(4/2008 — 7/2011)**
- Thesis: *Spatial parallelism in the routers of asynchronous on-chip networks* [27]
  - Designed and implemented asynchronous spatial division multiplexing (SDM) routers for asynchronous on-chip networks [25,26,29].
  - Designed and implemented a high-speed asynchronous wormhole router for asynchronous on-chip networks [31,33].
  - Designed and implemented the first asynchronous scheduler for three-stage S^3 Clos networks [28,30].
  - All designs are coded in synthesizable Verilog HDL (Faraday 130nm cell library), implemented by Synopsys DC-Topo, ICC, StarXRC, PrimeTime-PX, and simulated by SystemC/Verilog co-simulation using Cadence NC-Sim.

Beijing University of Technology, Beijing, P.R.China

September 2005 to September 2008
M.S.EE. in Automation, College of Electronic Information and Control Engineering

- Designed and implemented an ANSI C non-preemptive real-time scheduler [32,35,39,40] for the central controller of electrical vehicles. (supported by Beijing Sci. Foundation #KZ20041000501)

October 2004 to November 2006
Research Assistant, Beijing Embedded System Key Lab

- Implementing the ASIC prototypes into FPGA verification platforms for the final hardware test before tape out. FPGA platforms include Xilinx Virtex-4 and II. ASIC prototypes include the baseband for ATSC, DVB-T, DVB-C and WLAN 802.11g.

September 2001 to September 2005
B.S.EE. in Automation, College of Electronic Information and Control Engineering
Minor in Computer Science, College of Computer Science

PUBLICATIONS

[1] Wei He, Zhi Zhang, Yueqiang Cheng, Wenhao Wang, **Wei Song**, Yansong Gao, Qifei Zhang, Kang Li, Dongxi Liu, and Surya Nepal. **WhistleBlower: A system-level empirical study on RowHammer**. *IEEE Transactions on Computers*, accepted, 2023.

[2] 武延军, **宋威**, 张科, 邢明杰. RISC-V 技术及生态专题前言. 计算机系统应用, 2022, 31(9): 1–2.

[3] Sihao Shen, Da Xie, and **Wei Song**. **A new cross-platform memory safety test suite: Design and practice**. *Computer Systems & Applications*, Vol. 31, No. 10, pp. 39–49, October 2022.
沈思豪, 解达, **宋威**. 跨平台内存安全测试集设计. 计算机系统应用, 2022, 31(9): 39–49.

[4] Sihao Shen, Zhenzhen Li, and **Wei Song**. **Methods of extracting parameters of the processor caches**. In *Proceedings of the International Workshop on Security (IWSEC)*, Tokyo, Japan (hybrid), pp. 47–65, September 2022.

[5] **Wei Song** and Guangda Zhang. ***Asynchronous On-Chip Networks and Fault-Tolerant Techniques***. CRC press, Boca Raton, FL, United States, ISBN: 9781032255750, May 2022.

[6] **Wei Song**, Jiameng Ying, Sihao Shen, Boya Li, Hao Ma, and Peng Liu. **A comprehensive and cross-platform test suite for memory safety — Towards an open framework for testing processor hardware supported security extensions**. arXiv:2111.14072, November 2021.

[7] Zihan Xue, Da Xie, and **Wei Song**. **A new hardware performance counter based on RISC-V**. *Computer Systems & Applications*, Vol. 30, No. 11, pp. 3–10, November 2021.
薛子涵, 解达, **宋威**. 基于 RISC-V 的新型硬件性能计数器. 计算机系统应用, 2021, 30(11): 3–10.

[8] **Wei Song**, Boya Li, Zihan Xue , Zhenzhen Li, Wenhao Wang, and Peng Liu. **Randomized last level caches are still vulnerable to cache side-channel attacks! But we can fix it**. In *Proceedings of the IEEE Symposium on Security and Privacy (S&P)*, Online, pp. 955-969, May 2021.

[9] 张光达, **宋威**, 戴华东. 一种双轨信号异步传输链路系统. 中国发明专利, 申请号 201911392277.2, 专利号 CN111198838B, 2020.

[10] Xiaoxin Li, **Wei Song**, Xiaofei Fu, Lutan Zhao, Peinan Li, Rui Hou, and Dan Meng. **Remapped cache layout: Thwarting cache-based side-channel attacks with a hardware defense**. In *Proceedings of the CCF TCArch Bienneial Conference on Advanced Computer Architecture (ACA)*, Online, August 2020.
李小馨, **宋威**, 付霄飞, 赵路坦, 李沛南, 侯锐, 孟丹. 缓存布局重映射: 缓存侧信道攻击防御研究. CCF 全国计算机体系结构学术年会, 线上, 2020.

[11] **Wei Song** and Peng Liu. **Dynamically finding minimal eviction sets can be quicker than you think for side-channel attacks against the LLC**. In *Proceedings of the International Symposium on Research in Attacks, Intrusions and Defenses (RAID)*, Beijing, China, pp. 427–442, September 2019.

[12] Jun Zhang, Rui Hou, **Wei Song**, Sally A. McKee, Zhen Jia, Chen Zheng, Mingyu Chen, Lixin Zhang, and Dan Meng. **RAGuard: An efficient and user-transparent hardware machanism against ROP attacks**. *ACM Transactions on Architecture and Code Optimization*, Vol. 15, No. 4, pp. 50:1–50:21, January 2019.

[13] Jun Zhang , Rui Hou, **Wei Song**, Zhiyuan Zhan, Boyan Zhao, Mingyu Chen, and Dan Meng. **Stateful forward-edge CFI enforcement with Intel MPX**. In *Proceedings of the CCF TCArch Bienneial Conference on Advanced Computer Architecture (ACA)*, Yingko, Liaoning, China, August 2018.

[14] Jianping Zhu, **Wei Song**, Ziyuan Zhu, Jiameng Ying, Boya Li, Bibo Tu, Gang Shi, Rui Hou, and Dan Meng. **CPU security benchmark**. In *Proceedings of the 1st Workshop of Security-Oriented Designs of Computer Architectures and Processors (SecArch'18)*, Toronto, ON, Canada, pp. 8–14, October 2018.

[15] Guangda Zhang, **Wei Song**, Jim Garside, Javier Navaridas, and Zhiying Wang. **Handling physical-layer deadlock caused by permanent faults in quasi-delay-insensitive network-on-chip**. *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)*, Vol. 25, No. 11, pp. 3152-3165, November 2017.

[16] **Wei Song**, Dirk Koch, Mikel Luján, and Jim Garside. **Parallel hardware merge sorter**. In *Proceedings of International Symposium on Field-Programmable Custom Computing Machines (FCCM)*, Washington DC, United States, pp. 95–102, May 2016.

[17] Guangda Zhang, Jim Garside, **Wei Song**, Javier Navaridas, and Zhiying Wang. **Deadlock recovery in asynchronous networks on chip in the presence of transient faults**. In *Proceedings of International Symposium on Asynchronous Circuits and Systems (ASYNC)*, CA, United States, pp. 100–107, May 2015.

[18] Guangda Zhang, **Wei Song**, Jim Garside, Javier Navaridas, and Zhiying Wang. **Protecting QDI interconnects from transient faults using delay-insensitive redundant check codes**. *Microprocessors and Microsystems*, Vol. 38, No. 8, pp. 826–842, November 2014.

[19] Oriol Arcas Abella, Geoffrey Ndu, Nehir Sonmez,Mohsen Ghasempour,Adria Armejach, Javier Navaridas, **Wei Song**, John Mawer, Adrian Cristal, and Mikel Lujan. **An empirical evaluation of high-level synthesis languages and tools for database acceleration**. In *Proceedings of International Conference on Field Programmable Logic and Applications (FPL)*, Munich, Germany, pps. 8, September 2014.

[20] Guangda Zhang, **Wei Song**, Jim Garside, Javier Navaridas, and Zhiying Wang. **An asynchronous SDM network-on-chip tolerating permanent faults**. In *Proceedings of International Symposium on Asynchronous Circuits and Systems (ASYNC)*, Potsdam, Germany, pp. 9–16, May 2014.

[21] **Wei Song**, Guangda Zhang, and Jim Garside. **On-line detection of the deadlocks caused by permanently faulty links in quasi-delay insensitive networks on chip**. In *Proceedings of International Conference of the Great Lakes Symposium on VLSI (GLSVLSI)*, Houston, Texas, USA, pp. 211–216, May 2014.

[22] **Wei Song**, Jim Garside, and Doug Edwards. **Automatic data path extraction in large-scale register-transfer level designs**. In *Proceedings of IEEE International Symposium on Circuits and Systems (ISCAS)*, Melbourne, Australia, pp. 377–380, June 2014.

[23] **Wei Song** and Jim Garside. **Automatic controller detection for large scale RTL designs**. In *Proceedings of EUROMICRO Conference on Digital System Design (DSD)*, Santander, Spain, pp. 884–851, September 2013.

[24] Guangda Zhang, **Wei Song**, Jim Garside, Javier Navaridas, and Zhiying Wang. **Transient fault tolerant QDI interconnects using redundant check code**. In *Proceedings of EUROMICRO Conference on Digital System Design (DSD)*, Santander, Spain, pp. 3–10, September 2013.

[25] **Wei Song** and Doug Edwards. **Survey of asynchronous networks-on-chip**. *Journal of Computer-Aided Design & Computer Graphics*, Vol. 24, No. 6, pp. 699–709, 2012.
宋威, Doug Edwards. 异步片上网络研究综述. 计算机辅助设计与图形学学报, 2012, 24(6): 699–709.

[26] **Wei Song**, Doug Edwards, Jim Garside, and William J. Bainbridge. **Area efficient asynchronous SDM routers using 2-stage Clos switches**. In *Proceedings of Design, Automation & Test in Europe (DATE)*, Dresden, Germany, pp. 1495–1500, March 2012.

[27] **Wei Song**. ***Spatial Parallelism in the Routers of Asynchronous On-Chip Networks***. PhD Thesis, School of Computer Science, the University of Manchester, Manchester, UK, 2011.

[28] **Wei Song**, Doug Edwards, Zhenyu Liu, and Sohini Dasgupta. **Routing of asynchronous Clos networks**. *IET Computers & Digital Techniques*, Vol. 5, No. 6, pp. 452–467, 2011.

[29] **Wei Song** and Doug Edwards. **Asynchronous spatial division multiplexing router**. *Microprocessors and Microsystems*, Vol. 35, No. 2, pp. 85–97, 2011.

[30] **Wei Song** and Doug Edwards. **An asynchronous routing algorithm for Clos networks**. In *Proceedings of International Conference on Application of Concurrency to System Design (ACSD)*, Braga, Portugal, pp. 67–76, June 2010.

[31] **Wei Song** and Doug Edwards. **A low latency wormhole router for asynchronous on-chip networks**. In *Proceedings of Asia and South Pacific Design Automation Conference (ASP-DAC)*, Taipei, P.O.China, pp. 437–443, January 2010.

[32] 徐喆, 闫士珍, **宋威**, 余春暄, 段建民, 张明杰. 一种实现 CANopen 主站的方法. 中国发明专利, 申请号 200810056824.5, 专利号 CN101222510B, 2010.

[33] **Wei Song** and Doug Edwards. **Building asynchronous routers with independent subchannels**. In *Proceedings of International Symposium on SoC*, Tampere, Finland, pp. 48–51, October 2009.

[34] **Wei Song**, Doug Edwards, Jose Luis Nunez-Yanez, and Sohini Dasgupta. **Adaptive stochastic routing in fault-tolerant on-chip networks**. In *Proceedings of ACM/IEEE International Symposium on Networks-on-Chip (NoCS)*, San Diego, CA, USA, pp. 32–37, May 2009.

[35] Zhe Xu, Shizhen Yan, **Wei Song**, and Zhuo Zhang. **Development of the CANopen master based on MC9S12DP512 and μC/OS-II**. *Computer Engineering and Science*, Vol. 31, No. 5, pp. 118–120, 2009.
徐喆, 闫士珍, **宋威**, 张卓. 基于 MC9S12DP512 和μC/OS-II 的 CANopen 主站开发. 计算机工程与科学, 2009, 31(5): 118–120.

[36] Zhe Xu, Shizhen Yan, and **Wei Song**. **Object dictionary design of CANopen based on hash table**. *Computer Engineering*, Vol. 35, No. 8, pp. 44–46, 2009.
徐喆, 闫士珍, **宋威**. 基于散列表的 CANopen 对象字典的设计. 计算机工程, 2009, 35(8): 44–46.

[37] **Wei Song**. ***The Design and Implementation of a Master of the Application Layer of CANopen***. Master Dissertation, School of Electronic Information and Control Engineering, Beijing University of Technology, Beijing, P.R.China, 2008.
宋威. CANopen 现场总线应用层协议主站的开发与实现. 工学硕士学位论文, 电子信息与控制工程学院, 北京工业大学, 北京, 中国, 2008.

[38] **Wei Song**, Suiming Fang, Dan Yao, Lichao Zhang, and Cheng Qian. Clock synchronization in multi-FPGA designs. *Computer Engineering*, Vol. 34, No. 7, pp. 245–247, 2008.
宋威, 方穗明, 姚丹, 张立超, 钱程. 多 FPGA 的时钟同步. 计算机工程, 2008, 34(7): 245–247.

[39] **Wei Song**, Suiming Fang, Mingjie Zhang, and Zhe Xu. **Task scheduler in the design of CANopen master**. *Computer Measurement & Control*, Vol. 16, No. 4, pp. 558–560, 2008.
宋威, 方穗明, 张明杰, 徐喆. 任务调度在 CANopen 主站设计中的应用. 计算机测量与控制, 2008(16): 558–560.

[40] **Wei Song**, Shizhen Yan, Zhe Xu, and Suiming Fang. **Transplantable CANopen master based on non-preemptive task scheduler**. In *Proceedings of IEEE International Conference on Automation and Logistics (ICAL)*, Jinan, P.R.China, pp. 557–562, August 2007.

[41] **Wei Song** and Suiming Fang. Clock circuit design in FPGA based on BUFGMUX and DCM. *Modern Electronic Technique*, Vol. 29, No. 2, pp. 141–143, 2006.
宋威, 方穗明. 基于 BUFGMUX 与 DCM 的 FPGA 时钟电路设计. 现代电子技术, 2006, 29(2): 141–143.

[42] **Wei Song**. **FPGA Function Verification and Interface Design for the Baseband of IEEE 802.11g WLAN Network Card**. Bachelor Dissertation, School of Electronic Information and Control Engineering, Beijing University of Technology, Beijing, P.R.China, 2005.
宋威. **802.11g 无线网卡 Baseband 的 FPGA 验证和接口设计**. 学士毕业论文, 电子信息与控制工程学院, 北京工业大学, 北京, 中国, 2005.

[43] **宋威**. C 语言实现 MATLAB 6.5 中 M 文件的方法. 计算机与信息技术, 2004, 7(12): 57–58.

FUNDING

- **Research on the processor defense techniques against cache side-channel attacks**, National Natural Science Foundation of China, No. 62172406, Principal Investigator, 590,000 CNY, 01/2022–12/2025.
- **CAS pioneer hundred talents program**, Chinese Academy of Sciences, Principal Investigator, 2,000,000 CNY, 01/2021–12/2023.

- 内置安全处理器原型芯片系统研发, Beijing Municipal Science & Technology Commission, No. Z191100007119011, Researcher, 8,400,000 CNY, 05/2019–12/2019.
- **Research on the key hardware technologies of defending control-flow hijacking using on-chip tagged memory**, National Natural Science Foundation of China, No. 61802402, Principal Investigator, 240,000 CNY, 01/2019–12/2021.
- **CAS pioneer hundred talents program**, Chinese Academy of Sciences, Principal Investigator, 800,000 CNY, 06/2018–06/2020.
- 引进优秀青年人才, Institute of Information Engineering, Chinese Academy of Sciences, Principal Investigator, 500,000 CNY, 01/2018–12/2020.
- 软硬件协同的 SGX 安全架构的攻防研究与探索, Institute of Information Engineering, Chinese Academy of Sciences, Principal Investigator, 300,000 CNY, 12/2017–12/2018.
- **A open and collaborative approach to system-on-a-chip design**, UK Newton Fund, Co-Investigator, 50,000 GBP, 03/2016–12/2018.
- **lowRISC project**, private donation to the University of Cambridge, Researcher, 1,000,000 GBP, 11/2014–10/2017.
- **Continuous on-line adaptation in many-core systems: From graceful degradation to graceful amelioration**, UK EPSRC, No. EP/L000563/1, Researcher, 1,323,232 GBP, 09/2014–10/2014.
- **Advanced analytics for extremely large european databases**, EU Framework 7, No. 318633, Researcher, 3,746,410 EUR, 06/2013–09/2013.
- **Globally asynchronous elastic logic synthesis (GAELS)**, UK EPSRC, No. EP/I038306/1, Researcher, 411,043 GBP, 10/2011–03/2015.
- **Energy efficient networks-on-chip for dynamically reconfigurable computing platforms**, UK EPSRC, No. EP/E06065X/1, Student Researcher, 319,957 GBP, 04/2008–07/2011.
- **Doctoral training award – the University of Manchester**, UK EPSRC, No. EP/P503833/1, full PhD scholarship, 10/2007–03/2011.
- Bursary of the School of Computer Science, University of Manchester, 10/2007–3/2011.

ACADEMIC ACTIVITIES

ACM (member: 2021–, SIGSAC member: 2021–);
CCF (member: 2017–, TFICD member: 2020–);
CRVA (individual member: 2019–);
IEEE (member: 2012–, computer society member: 2021–, student member: 2008–2011);
RVI (community individual member: 2020–, lowRISC: 2016–2017).

Program Committee member for:
RVTE (RISC-V 技术及生态研讨会): 2021–2023
IEEE/IFIP International Conference on Dependable Systems and Networks (DSN): 2022
RISC-V World Conference China (RISC-V 中国峰会): 2022, 2021
CRVA Technical Seminar (CRVA 联盟技术研讨会): 2020
China RISC-V Forum (中国 RISC-V 论坛): 2019
CCF TCArch Bienneial Conference on Advanced Computer Architecture (ACA): 2018

Organizer Committee member for:
IEEE Interational Symposium on Asynchronous Circuits and Systems (ASYNC): local arrangement chair 2023

Guest Editor for:
Computer Systems & Applications (计算机系统应用)
Cybersecurity

Reviewer for:
Chinese High Technology Letters (高技术通讯)
Computer Engineering & Science (计算机工程与科学)
EURASIP Journal on Embedded Systems
IEEE Communications Letters
IEEE Micro
IEEE Transactions on Dependable and Secure Computing
IEEE Transactions on Parallel and Distributed Systems
IET Computer and Digital Techniques
Journal of Computers
Journal of Cyber Security (信息安全学报)
Journal of Parallel and Distributed Computing
Microprocessors and Microsystems

Other:
Editor for *CNRV Bi-Weekly News*

TEACHING EXPERIENCE

School of Cyber Security, University of Chinese Academy of Sciences (UCAS), Beijing, P.R. China

Lecturer

- *Computer Architecture Security*, 1st year Master, 2019–2023.
- *Digital Circuits*, 2nd year undergraduate, 2019–2022;
  2021's excellent undergraduate course in both UCAS and the School of Cyber Security.

Computer Laboratory, the University of Cambridge, Cambridge, UK

Lab Demonstrator

- *ECAD and Architecture Practical Classes*, Part IB (2nd year undergraduate), 2016.

Supervisor (small group tutor)

- *Comparative Architectures*, Part II (3rd year undergraduate), 2016, 2017.
- *System-on-Chip Design*, Part II (3rd year undergraduate), 2016, 2017.

School of Computer Science, the University of Manchester, Manchester, UK

Graduate Student Lab Demonstrator

- *Microcontrollers*, 2nd year undergraduate, 2008, 2013.
- *Fundamentals of Computer Engineering*, 1st year undergraduate, 2010.
- *VLSI System Design*, 2nd year undergraduate, 2007–2010.
- *Fundamentals of Computer Architecture*, 1st year undergraduate, 2008–2010.
- *Mobile Systems*, 2nd year undergraduate, 2010.
- *Operating Systems*, 2nd year undergraduate, 2009.

STUDENTS

Current Students

- *Zihan Xue* (薛子涵): IIE/UCAS, PhD 2019
- *Zhenzhen Li* (李真真): IIE/UCAS, PhD, 2019
- *Da Xie* (解达): IIE/UCAS, PhD, 2020
- *Hao Ma* (马浩): IIE/UCAS, PhD, 2020
- *Wei He* (何玮): IIE/UCAS, PhD, 2022 (with Prof. Wenhao Wang)
- *Ciyan Ouyang* (欧阳慈俨): IIE/UCAS, PhD, 2022
- *Xiuwei Pang* (庞修微): IIE/UCAS, Master, 2020
- *Jinchi Han* (韩金池): IIE/UCAS, Master, 2022
- *Zhidong Wang* (王智栋): IIE/UCAS, Master, 2023
- *Boyuan Pang* (庞博远): UCAS, undergraduate, 2020
- *Zengtao Yang* (杨锃涛): UCAS, undergraduate, 2021

Graduated

- *Sihao Shen* (沈思豪): IIE/UCAS, Master 2022 → T-head.
- *Mingyu Huang* (黄铭宇): UCAS, Bachelor 2022.
- *Boya Li* (李博雅): IIE/UCAS, Master 2021 → Cambricon.
- *Bangya Liu* (刘邦亚): HUST, Bachelor 2019 → PhD @ Univ. of Wisconsin-Madison.

Advised

- *Yingjie Zhang* (张英杰): UCAS, undergraduate student 2019–2022, → PhD @ IIE/UCAS.
- *Peng Wang* (王鹏): UCAS, PhD student 2019–2020, transferred to SIAT/UCAS.
- *Jiahao Ma* (马家豪): Xidian Univ., Master 2020 → Cambricon.
- *Xiaofei Fu* (付霄飞): Xidian Univ., Master 2019 → VeriSilicon.
- *Hongyan Xia*: Univ. of Cambridge, MPhil 2015 → PhD @ Univ. of Cambridge.
- *Martin Papadopoulos*: Univ. of Cambridge, MPhil 2015 → PwC.

OPEN-SOURCE PROJECTS

CPU-Sec-Bench usable (2018–present): lead, security test benchmark for computer architectures.
https://github.com/comparch-security/cpu-sec-bench

Spike-Cache usable (2019–present): Spike incorporated with the new cache model.
https://github.com/comparch-security/spike-cache

Cache-Model usable (2018–present): A C++ implemented fast cache model.
https://github.com/comparch-security/cache-model

Smart-Cache-Evict stable: A set of C++ implemented fast eviction set search algorithms inspired by and improved from Pepe Vila's algorithm.
https://github.com/comparch-security/smart-cache-evict

FPGA-Rocket-Chip usable: Yet another attempt to port the latest Rocket-Chip (2018) to a Nexys4-DDR board.
https://github.com/cnrv/fpga-rocket-chip

Rocket-Chip-Read stopped: Commenting the deplomacy and TileLink packages used in the Rocket-Chip project around 2016 to 2017.
https://github.com/cnrv/rocket-chip-read

lowRISC member (2014–2017): Providing an open-source SoC platform using the 64-bit RISC-V ISA.
https://github.com/lowrisc/lowrisc-chip

Open-SoC-Debug contributor (2015–2016): Providing building blocks for SoC debug systems.
https://github.com/opensocdebug

Asynchronous Verilog Synthesiser beta, developing stopped: Generate elastic or asynchronous circuits from synchronous RTL designs written in Verilog HDL.
https://github.com/wsong83/Asynchronous-Verilog-Synthesiser

cppSaif stable: A C++ library for parsing SAIF (Switching Activity Interchange Format) files.
https://github.com/wsong83/cppSaif

C++/Tcl stable: A C++ library for interoperability between C++ and Tcl.
Adopted from the original C++/Tcl designed by Maciej Sobczak.
https://github.com/wsong83/cpptcl

VPreproc stable: A standalone C++ preprocessor for the Verilog HDL language.
Adopted from the Verilog Perl tool suite designed by Wilson Snyder.
https://github.com/wsong83/vpreproc

Asynchronous Spatial Division Multiplexing (SDM) Router stable: Hardware designs of asynchronous SDM routers using Nangate 45nm cell library. Gate-level, synthesisable netlist written in Verilog HDL. SystemC testbenches and synthesis scripts for Synopsys DC provided.
https://github.com/wsong83/qdi-sdm-noc
http://opencores.org/project,async_sdm_noc

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