System-on-Chip Design Supervision Problem (Set 3)

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You can draw diagrams if feel necessary but using Verilog is preferred. Please keep your answers organised and tidy. If you could not answer some questions or would like a discussion during the supervision session, please label it in your answer.

SP 6. ESL and TLM

Q1: Briefly explain how and why an ESL model that uses a TLM model of its buses can run the embedded software with no modification to its device drivers.

Q2: Explain how the device driver for an on-chip network might be modified if the network devices itself is not to be modelled and instead transactions are to be used to directly pass packets between network nodes.

Q3: What is the difference between a blocking and non-blocking transaction in terms of implementation, efficiency and callability?

Q4: Sketch a SystemC code for a shim function that converts a transactional port from blocking to non-blocking.

Q5: What is the advantage of putting a reference-passed delay parameter in a TLM call?

Q6: Consider what simulation performance an ISS might give and can it ever be faster than real time?

Q7: Briefly describe each of: cycle-accurate, approximately timed, loosely timed and untimed.

Q8: What is the purpose and effect of the timing quantum in the loosely-timed model? Why might a transactional system exhibit different behavior as the quantum is adjusted?

Q9: How can contention for a resource be modeled with and without actual queuing of the transaction?

Extra. Past exam

(a) Explain what factors limit the complexity and performance of an SoC at the heart of a portable electronic device. [4 marks]

(b) Compare and contrast the use of hardware and software to implement a compute-intensive algorithm on an SoC, such as data encryption. Include customised processors and co-processors in your analysis. [5 marks]

(c) (i) Define the term fully-pipelined with respect to a hardware component. [2 marks]

(ii) Describe and compare three designs for a fixed or floating-point multiplier that vary in performance: one at least should be fully pipelined. [6 marks]

(iii) Define the term structural hazard and explain why these can affect system performance. Which of your designs from part(c)(ii) might present such a hazard and why? [3 marks]