System-on-Chip Design Supervision Problem (Set 1)

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You can draw diagrams if feel necessary but using Verilog is preferred. Please keep your answers organised and tidy. If you could not answer some questions or would like a discussion during the supervision session, please label it in your answer.

SP 1. SoC Components and Bus Structure

Q1: Wire up a push button to a GPIO pin and describe the action of (or sketch out the code for) a device driver that sets up the GPIO device and returns how many times it has so far been pressed. Describe firstly the polling code. Then write a few sentences about how the interrupt driven solution would be implemented and when it should be used instead. [SoC-SP1.4]

Q2: Sketch RTL Verilog code for a 3-input non-preemptive static prioritized arbiter. Then extend it into a non-preemptive round-robin arbiter. [Optional] How can we make the arbiter to support up to N inputs, where N is a design time parameter? [Extended SoC-SP1.15]

SP 3. SoC Busses, Partition and Technology

Q3: Consider multiple busses with bridges [SoC-SP3.2]:

1. In current SoCs, what is a bus and how does it compared with the 1980's concept of a motherboard bus (such as ISA or PCI bus)?
2. How might the destination port for a transaction over such a bus be decided?
3. What is a bus bridge, what transactions might it support and what internal operations might it implement?
4. If a SoC is designed with a number of bridged busses, what are the main aspects that determine the allocation of initiators and targets to the bus?
5. What is the difference between a network-on-chip (NoC) and multiple bridged busses?
6. What form of bus protocol is needed for good performance on a SoC that uses a number of bridged busses or clock domains?
7. How is contention for destinations handled in a SoC that uses a number of bridges busses compared with a NoC?

Q4: DRAM and cache [SoC-SP3.4]:

1. Why is DRAM not commonly integrated in the same die as a part of a SoC?
2. Considering accesses to DRAM, why should out-of-order read responses ideally be supported by a SoC bus or NoC?

Q5: Cell library [SoC-SP3.6]:

1. Give a short list of logic cells found in a standard cell library.
2. List five types of information that should be stored for each cell in a library.
3. [Optional] When estimating the latency of a gate (implemented using a standard cell) in a circuit, what information stored in the cell library is related and what is the relationship (no equation needed)?

SP 3. Silicon Energy, Power and Technology

Q6: Dynamic voltage and frequency scaling [Power.3]:

1. Give a formula for estimating the dynamic power dissipation related to supply voltage, capacitance, and clock frequency.
2. What is dynamic clock gating and compare this to a technique where software writes to a control register that turns off a clock generator.
3. For a fixed supply voltage, quantify the power benefits of frequency scaling.
4. Give two ways that the supply voltage to a region may be varied.
5. Using variable supply voltage, quantify the power benefit of frequency scaling.