2020-2021学年秋季学期

第七部分
可编程逻辑电路

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可编程逻辑电路

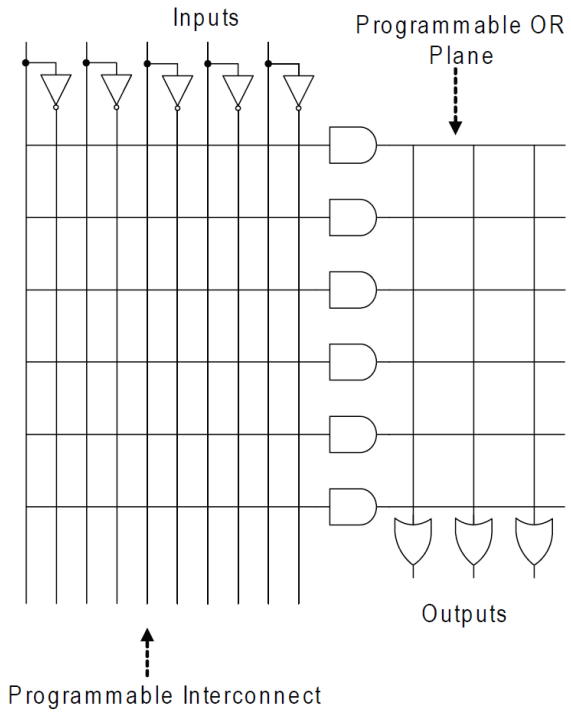
可编程逻辑电路是一种半定制的大规模集成电路，允许电路在生产完成之后，通过配置，实现用户所需要的逻辑功能。

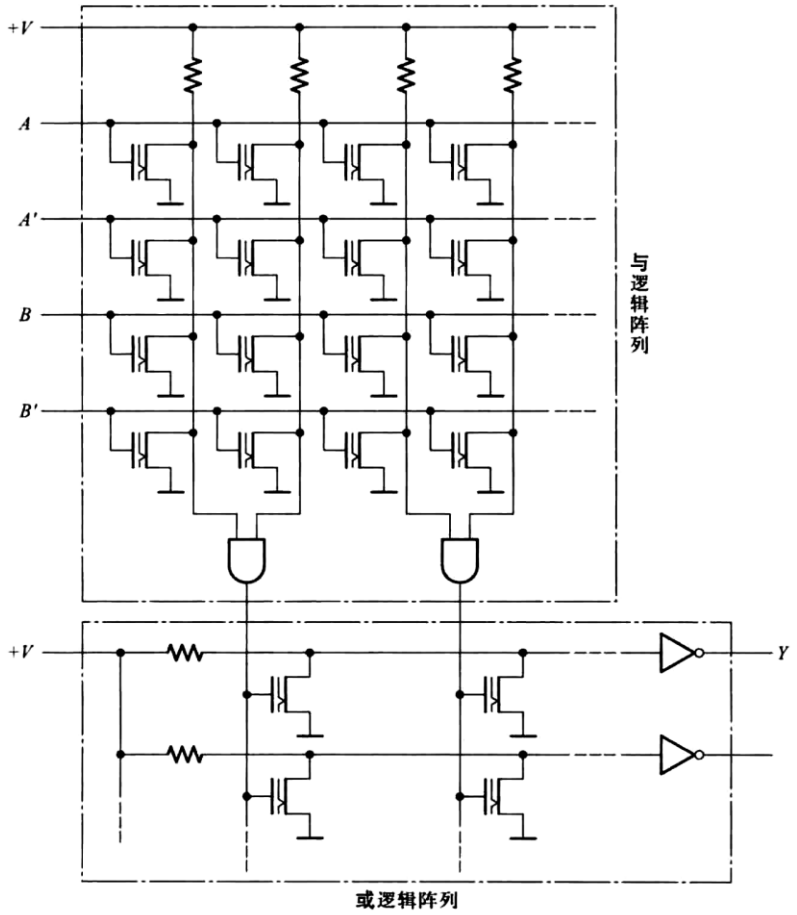
从简单到复杂，可编程逻辑电路分为：

- **PLA（programmable logic array）**
  - 由可编程逻辑阵列，与门和或门构成的可编程电路
  - 实现组合逻辑
- **PAL（programmable array logic）**
  - 在PLA的基础上添加D-FF，可用于实现时序逻辑
- **CPLD（complex programmable logic device）**
  - 大规模PAL阵列
- **FPGA（field programmable gate array）**
  - 使用更高密度的可编程逻辑阵列（传输门）和配置存储（SRAM）

PLA

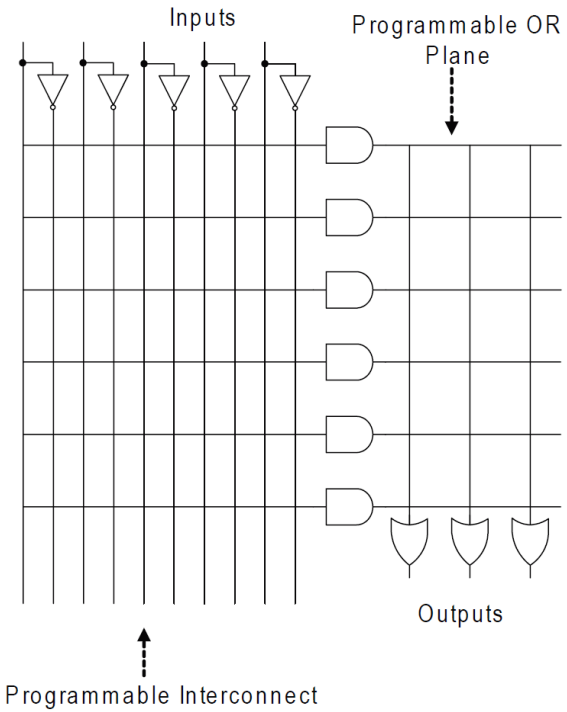
- 由可编程逻辑阵列，与门和或门构成的可编程电路
- 实现组合逻辑



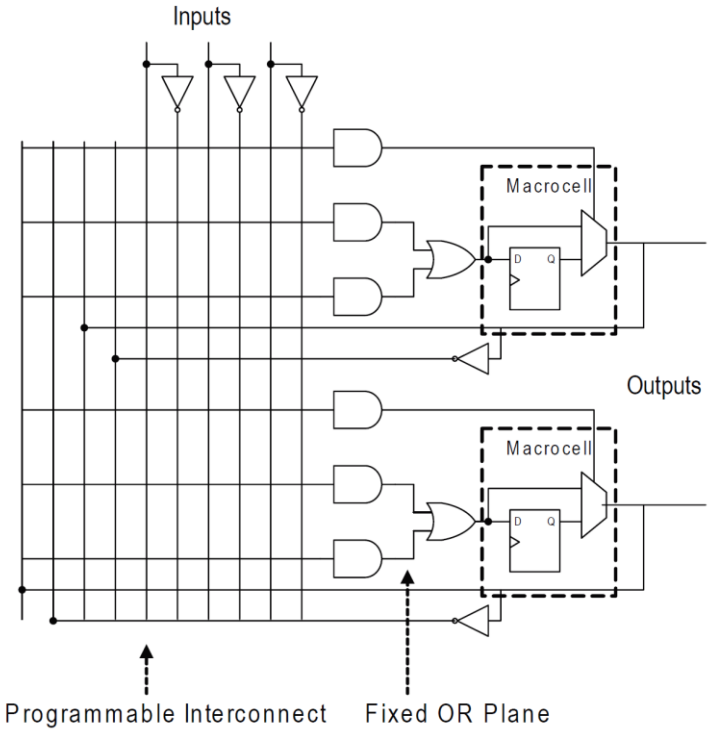


PAL

- 在PLA的基础上，添加带DFF的宏单元（macrocell）
- 实现时序逻辑



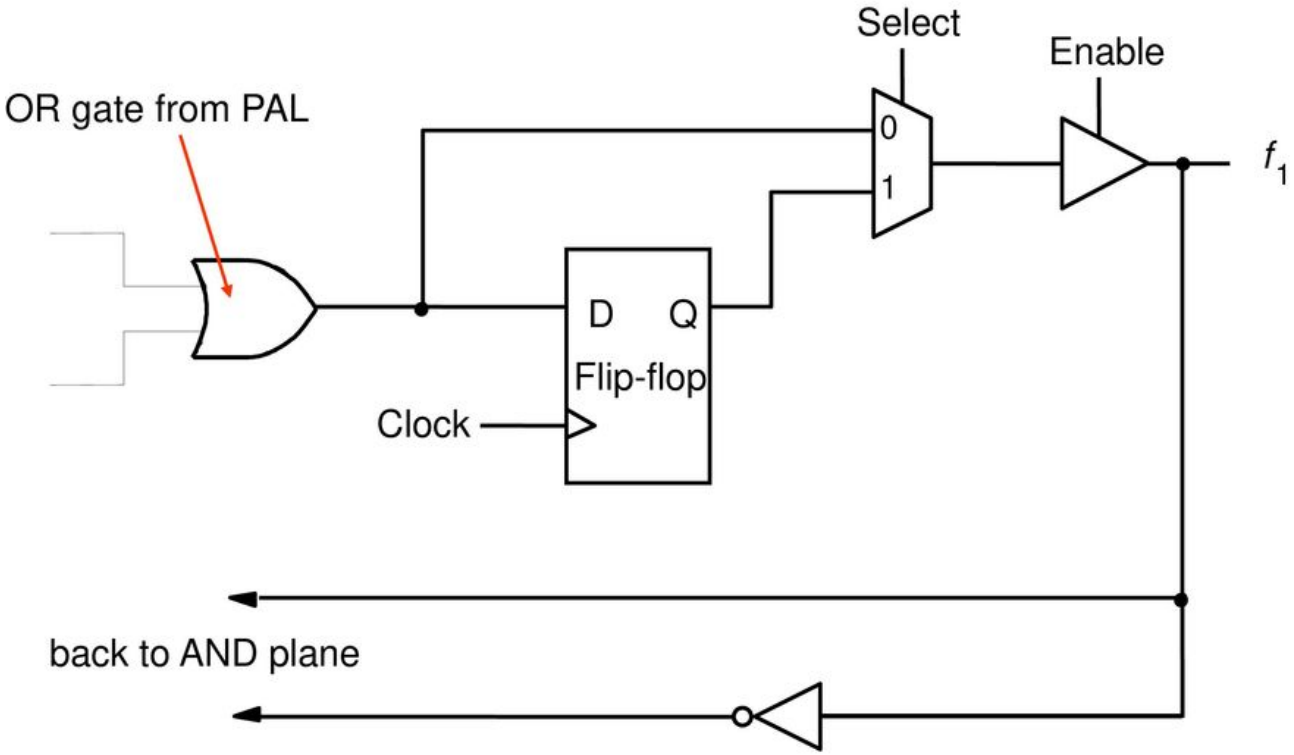
PLA



PAL

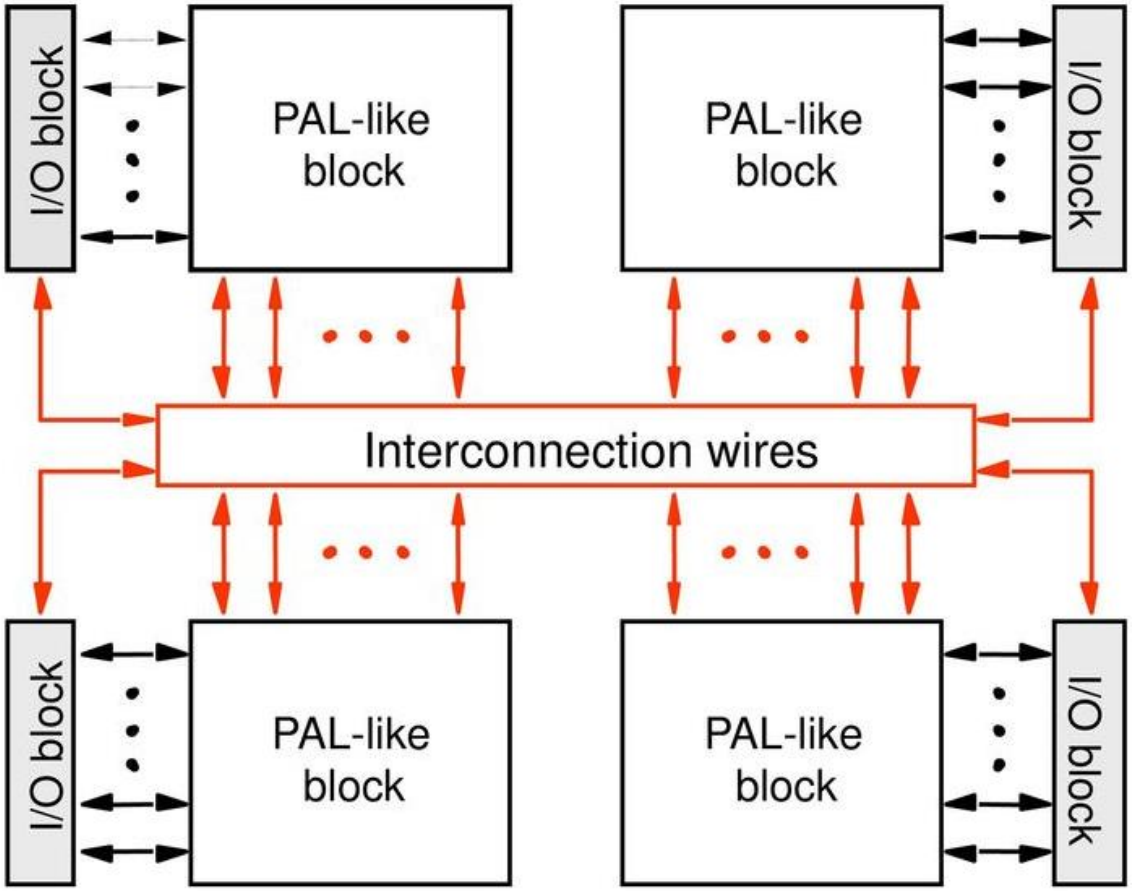
MacroCell

- 包含DFF，作为状态保持单元
- 包含选择器和三态门，可以作为一般/三态输出
- 包含回馈逻辑，返回状态给PLA的组合逻辑阵列

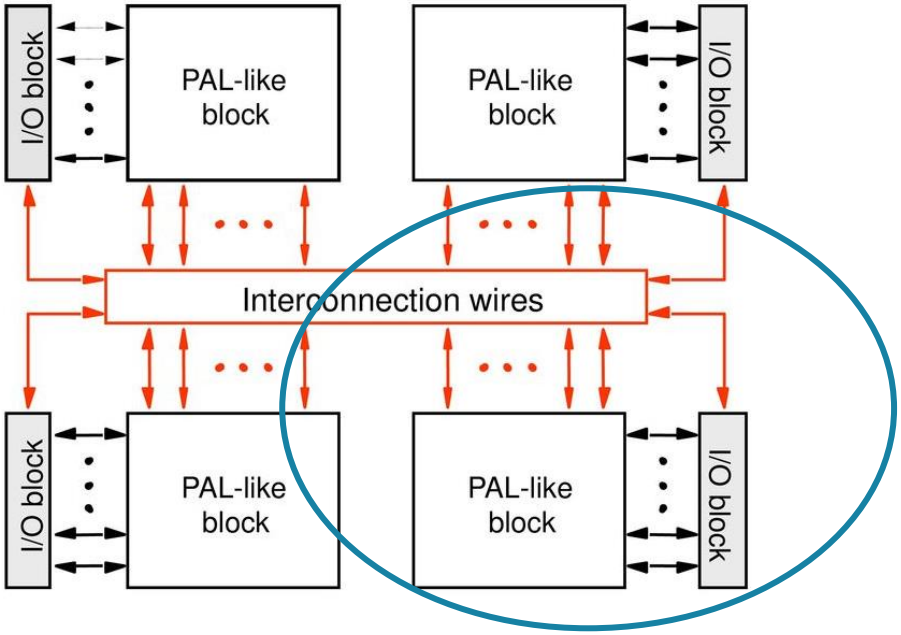


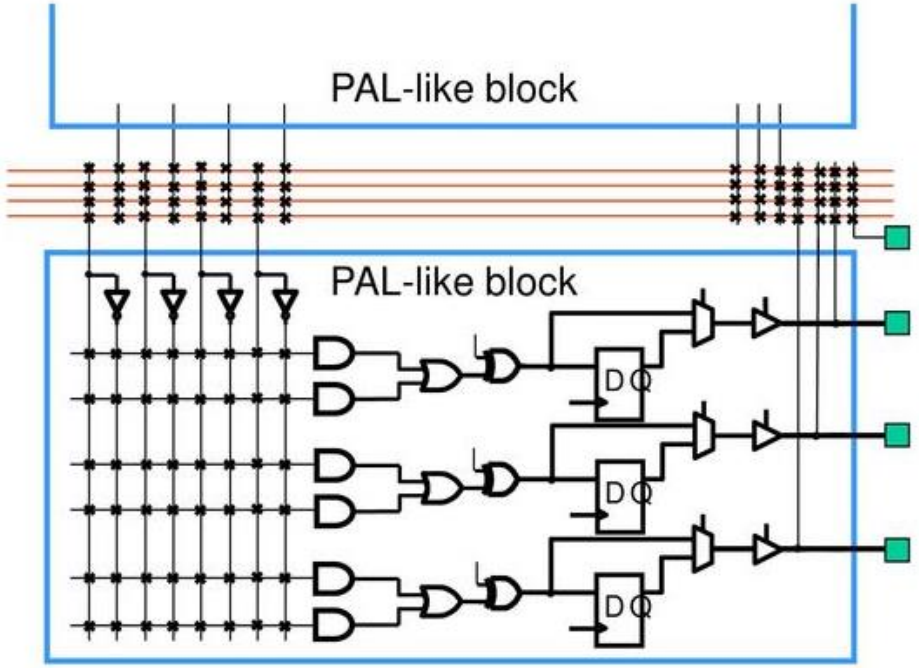
CPLD

- 包含多个PAL模块的可编程逻辑器件
- PAL模块间用片上互联网络连接



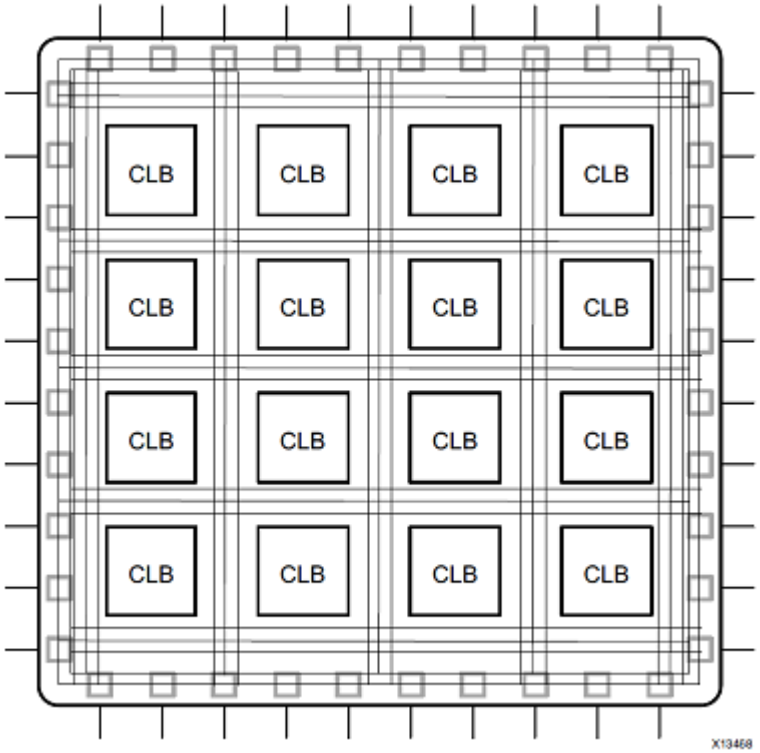
CPLD


I/O block
PAL-like block
PAL-like block
I/O block
Interconnection wires
I/O block
PAL-like block
PAL-like block
I/O block


PAL-like block
PAL-like block
D Q
D Q
D Q

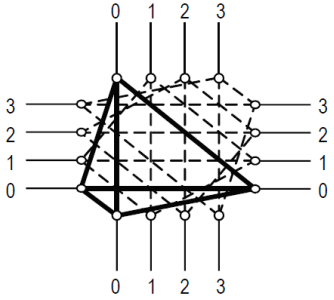
FPGA

- FPGA由众多可编程逻辑块（CLB）构成
- CLB之间通过可编程的连接网络连接
- 与CPLD不同的是，FPGA的可编程开关由SRAM驱动
  - 上电需要配置，掉电丢失，但是面积代价小

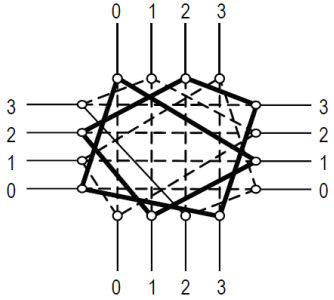


FPGA的连接网络

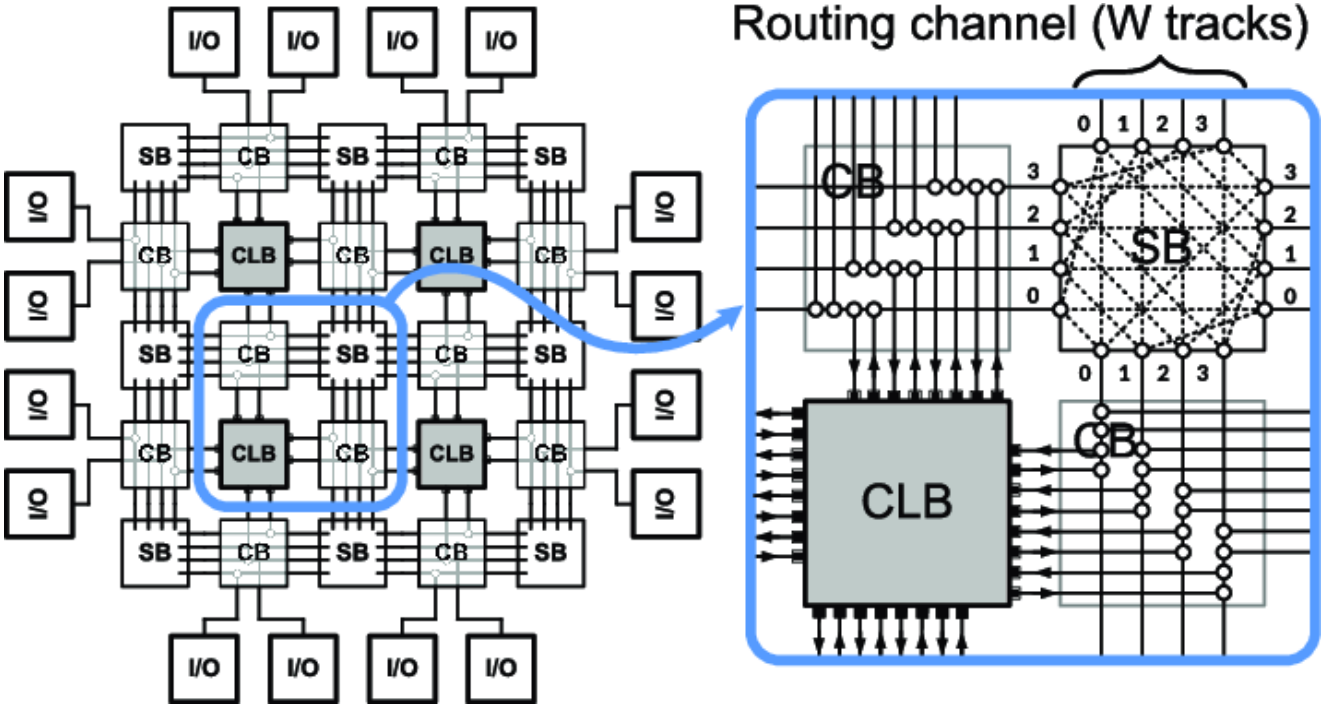
- CB：connection block，固定连接
- SB：switching block，可配置连接



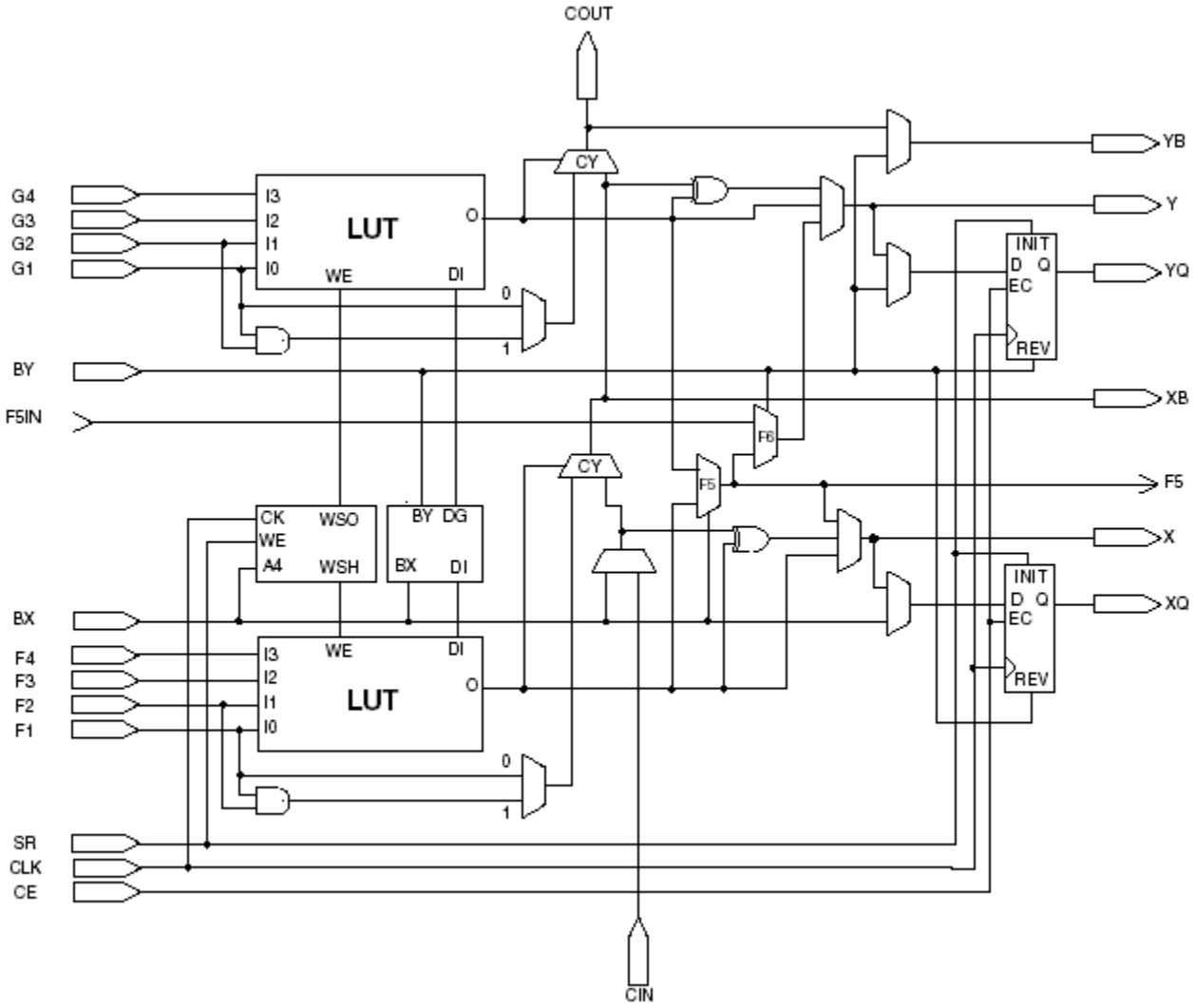
(a) Disjoint



(b) Wilton

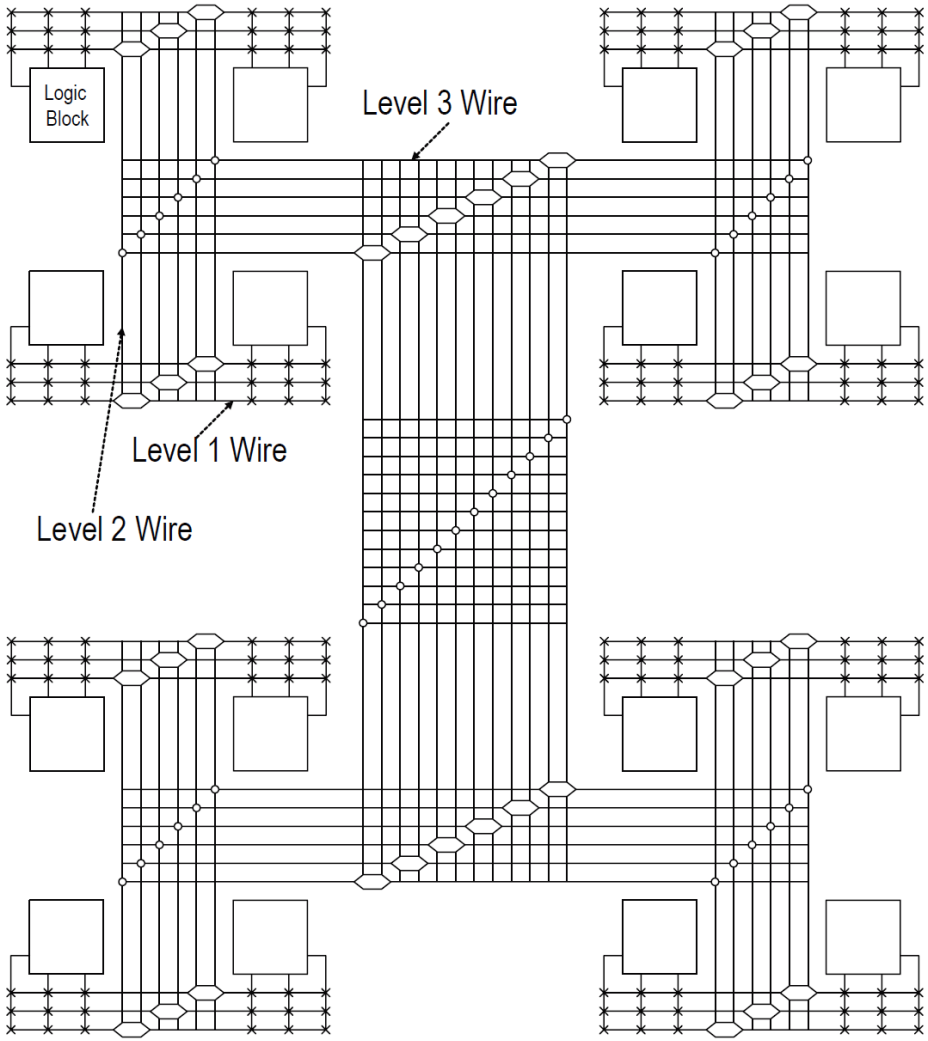


FPGA的CLB


COUT
CY
YB
Y
G4
G3
G2
G1
I3
I2
I1
I0
LUT
O
WE
DI
0
1
INIT
D Q
EC
REV
YQ
BY
XB
F5IN
F6
CY
F5
F5
CK
WE
A4
WSO
WSH
BY DG
BX DI
X
INIT
D Q
EC
REV
XQ
BX
F4
F3
F2
F1
I3
I2
I1
I0
LUT
WE
DI
O
0
1
SR
CLK
CE
CIN

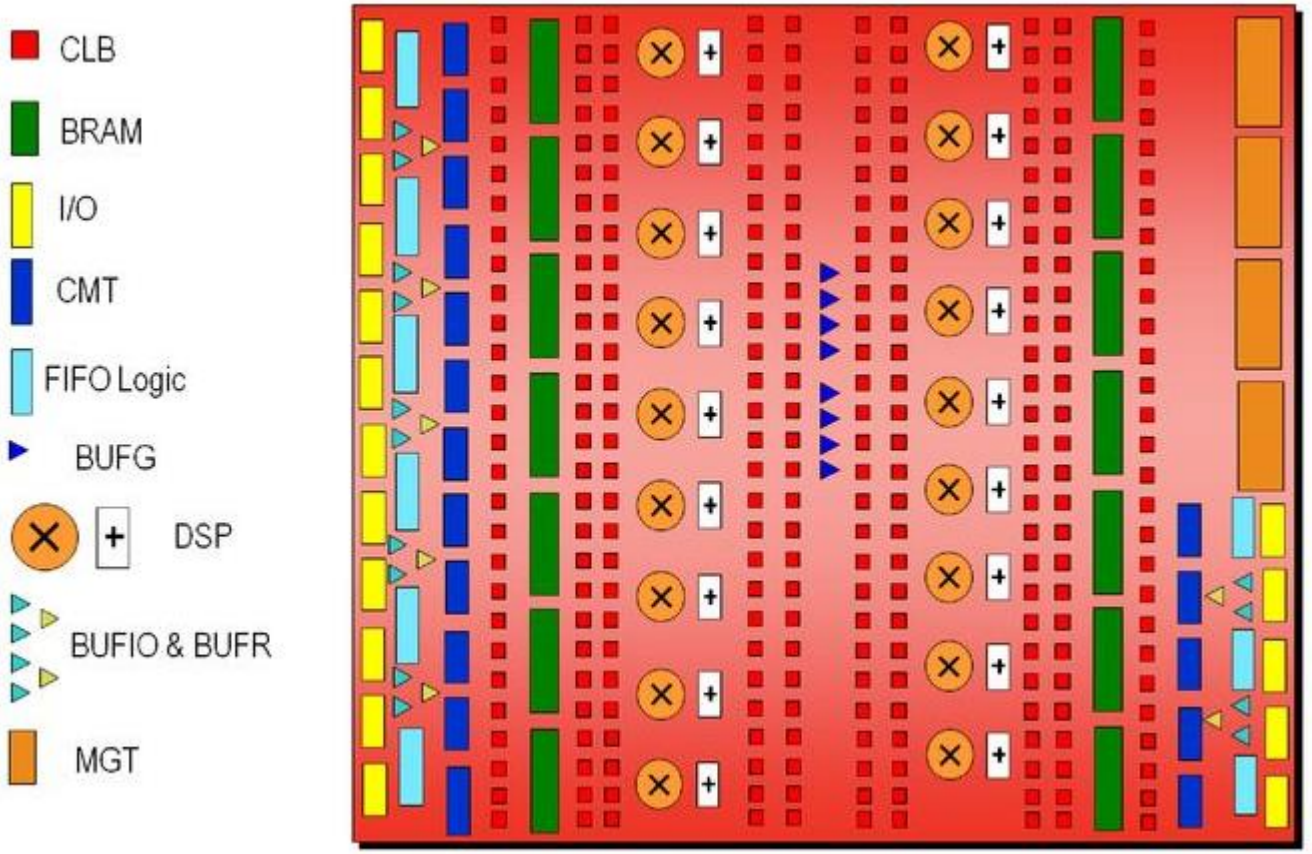
更大的FPGA

- 更大的FPGA需要用Hierarchical的结构连接



FPGA的内部资源

- 更复杂的FPGA包含多种异质IP



FPGA的配置

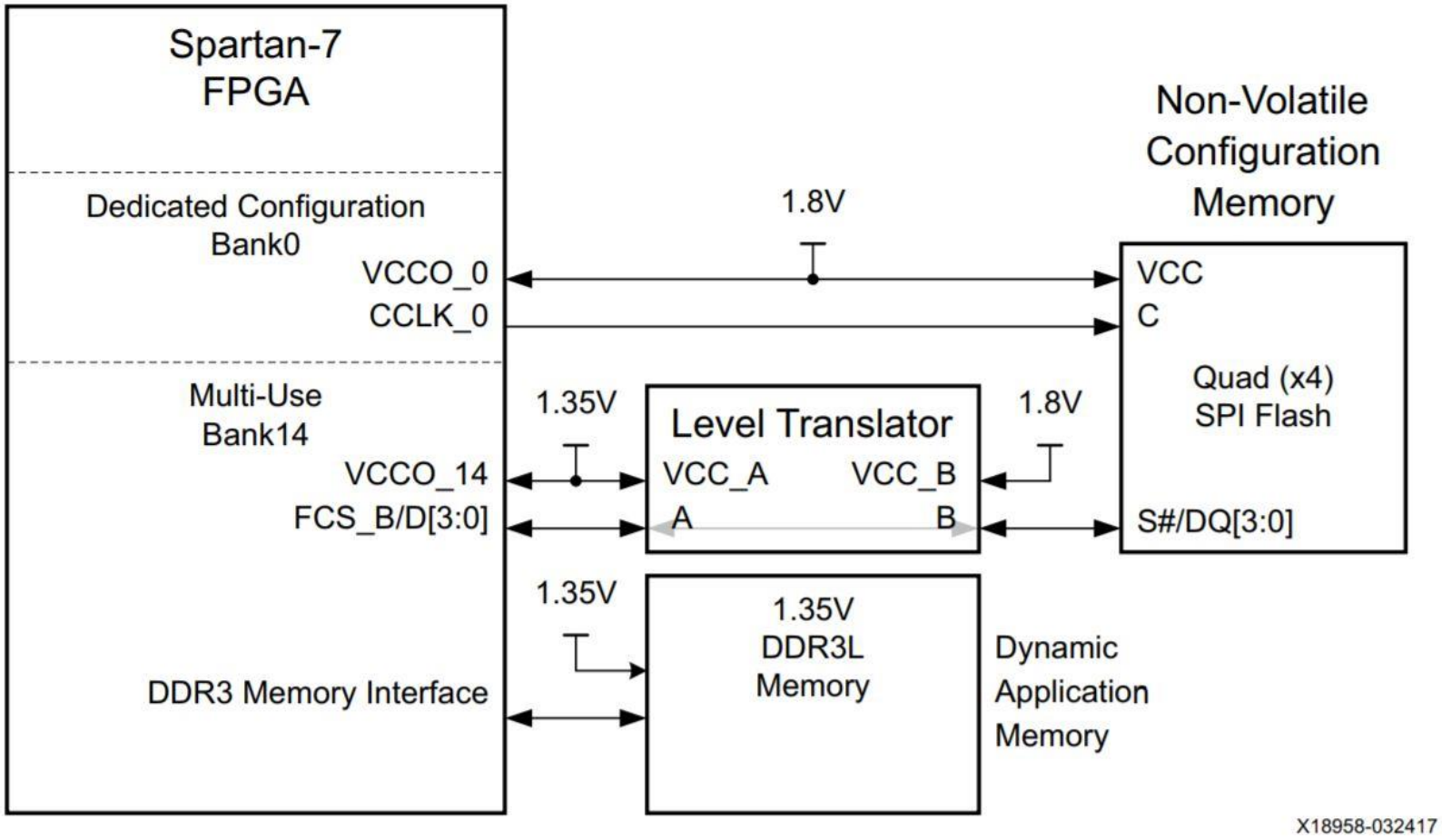
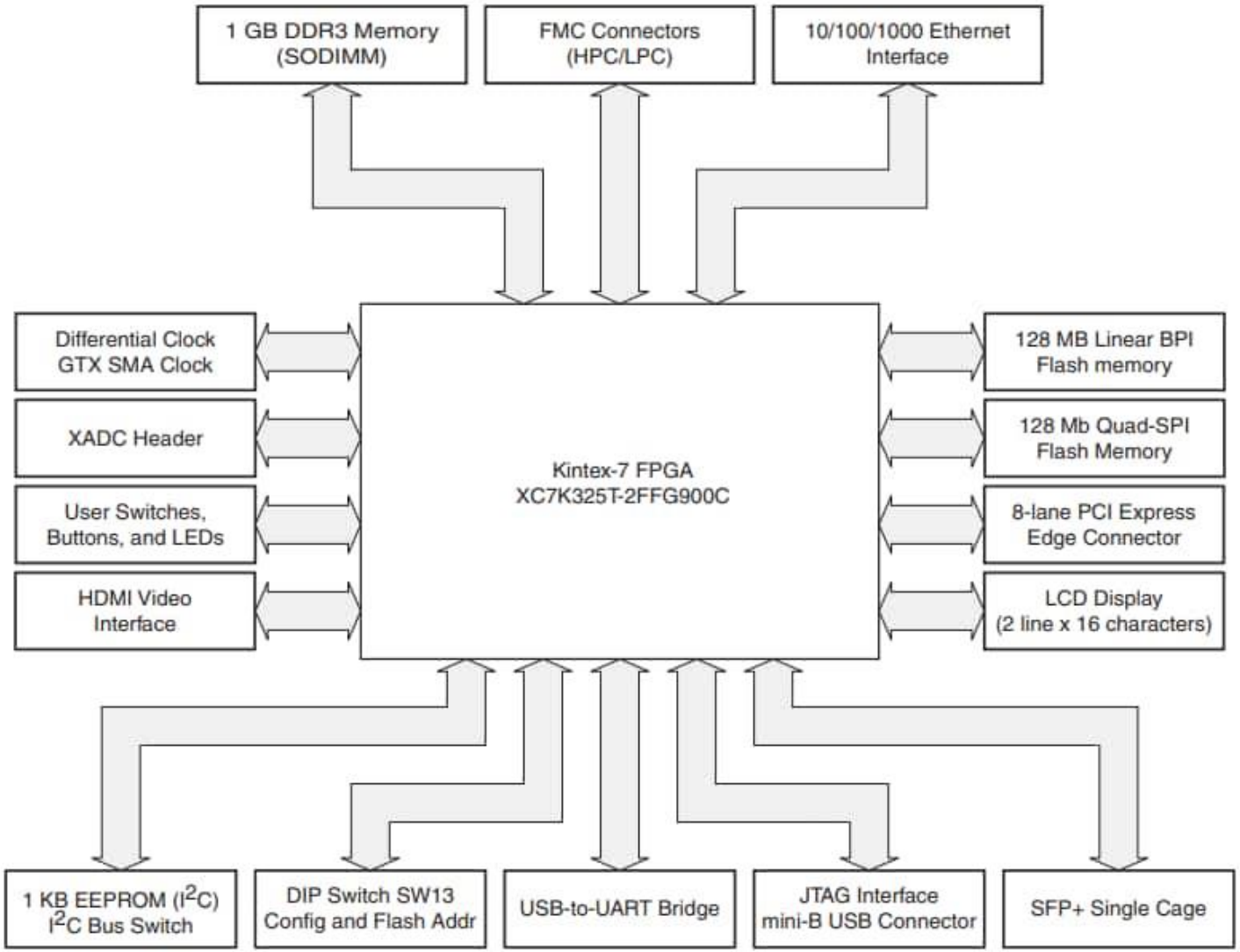
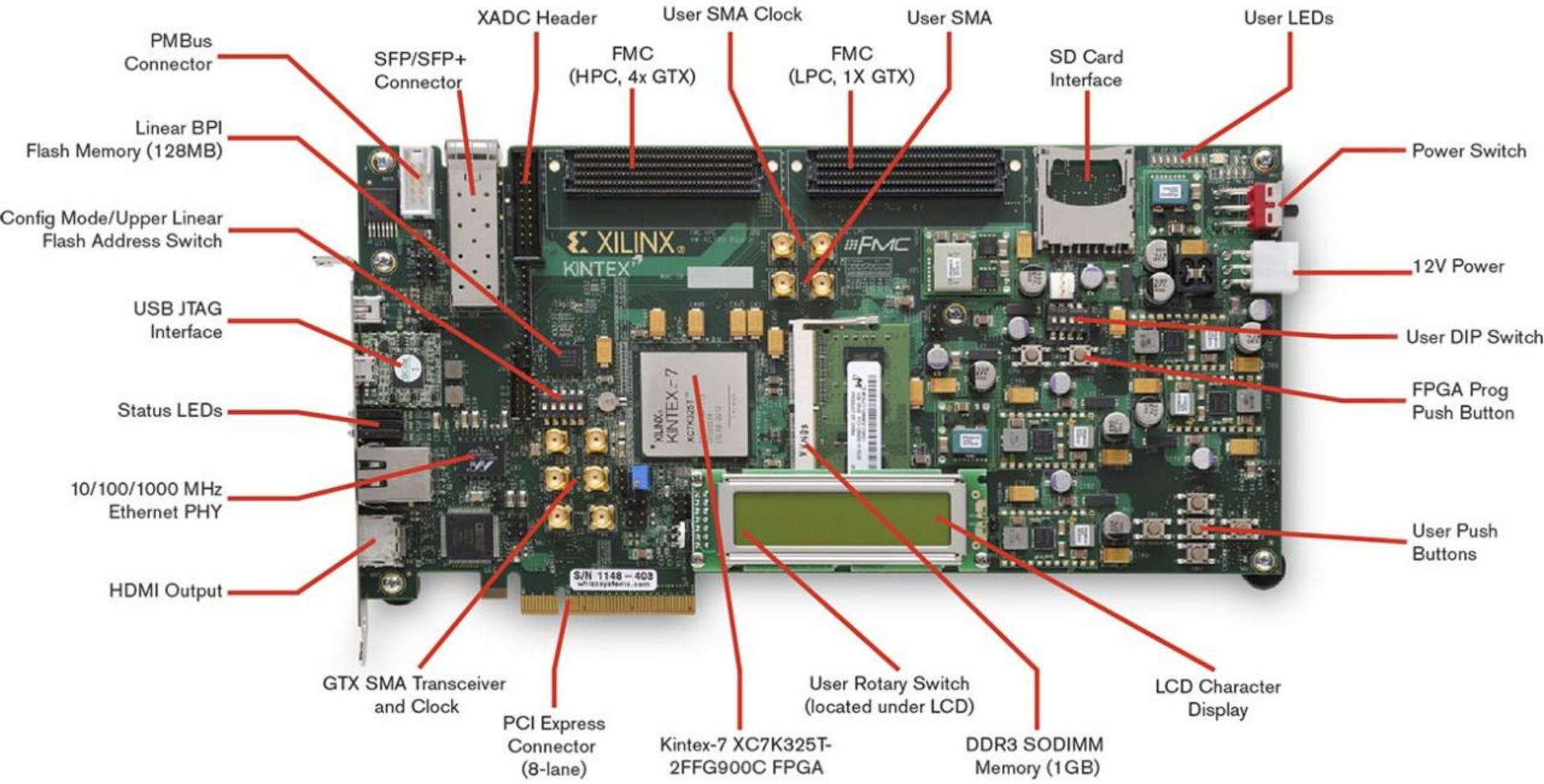


Figure 1: **Spartan-7 FPGA with 1.8V SPI Configuration Flash and 1.35V DDR3L**

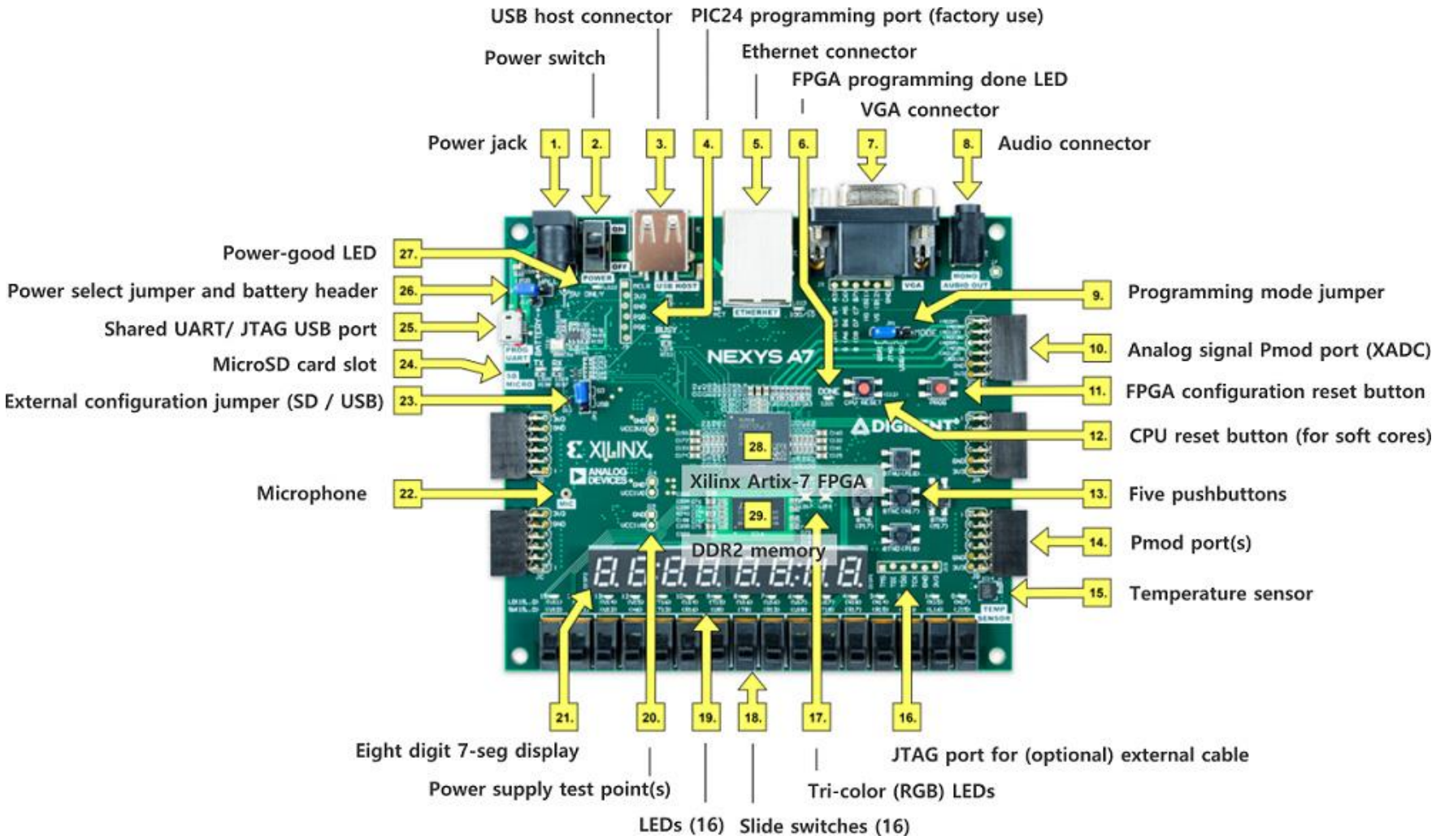
FPGA开发板（Xilinx KC705）



FPGA开发板（Xilinx KC705）



FPGA demo (Nexys4-DDR)



总结：考试范围（概念）

- 可编程逻辑电路
  - 半定制，可编程
  - CPLD和FPGA的区别
  - FPGA的配置

任何问题?

课堂习题（提问方式）

- FPGA和ASIC相比的优缺点比较。