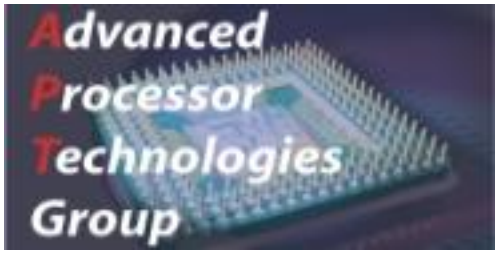

Improving the Throughput of Asynchronous On-chip Networks with SDM

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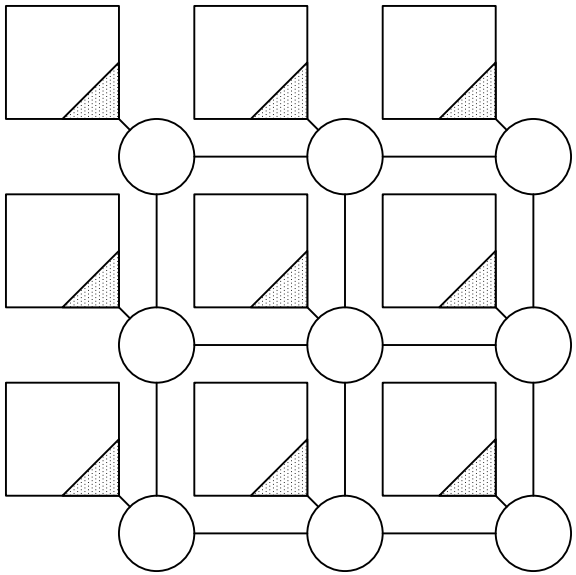
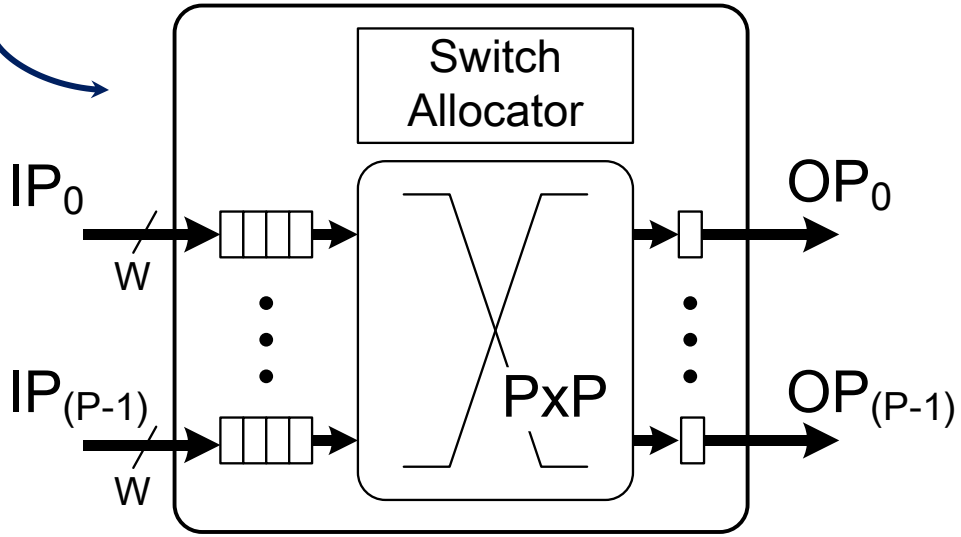
Outline

- Introduction
  - Network-on-Chips (NoCs)
  - Flow control: wormhole, virtual channel (VC) and spatial division multiplexing (SDM)
- SDM router
  - Implementation
  - Area and speed model
- Speculation of a VC router
  - Area and speed model
- Performance analysis
  - Latency accurate SystemC models

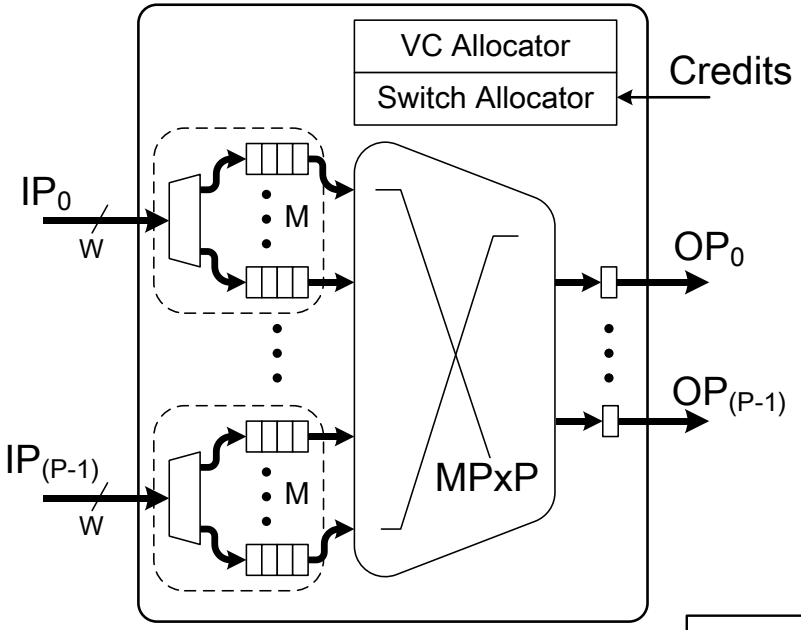
Network-on-Chips



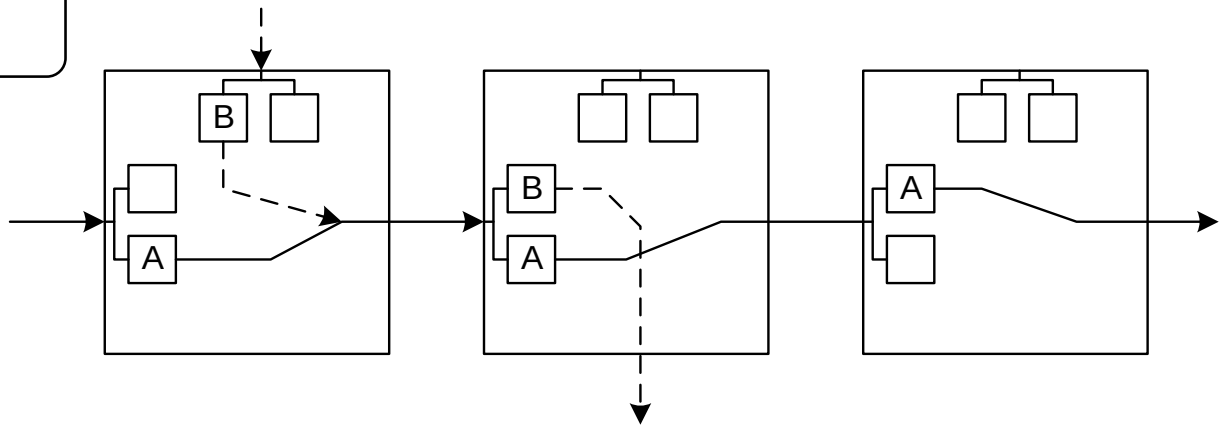


wormhole

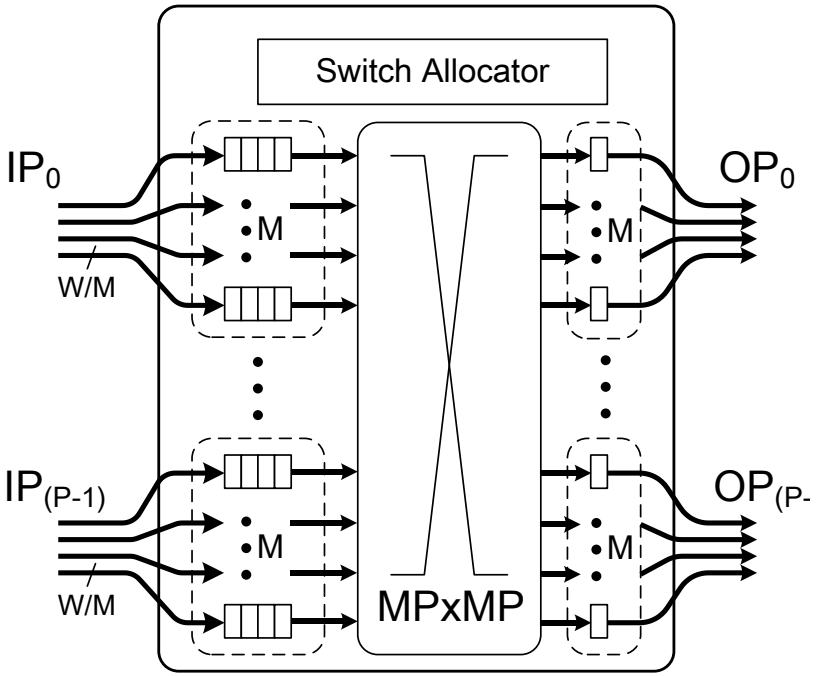
Virtual Channel (VC)

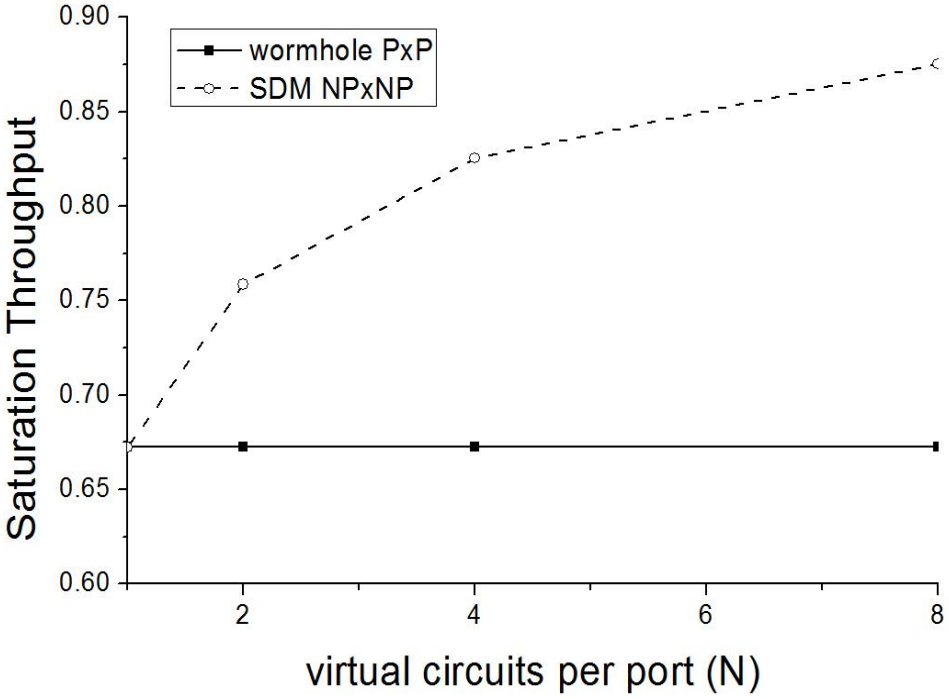


Blocked flits are buffered in virtual channels; therefore, links are available to other flits.



Spatial Division Multiplexing (SDM)





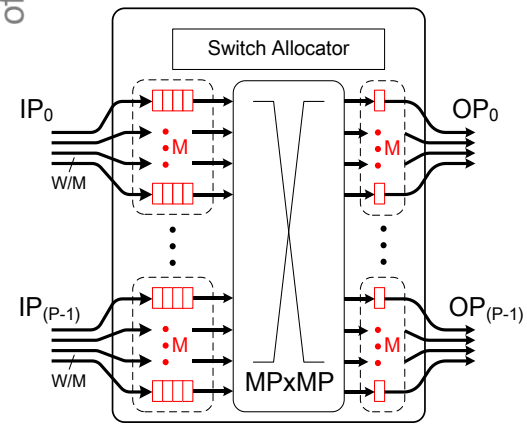
$th_{wormhole} = 0.67$

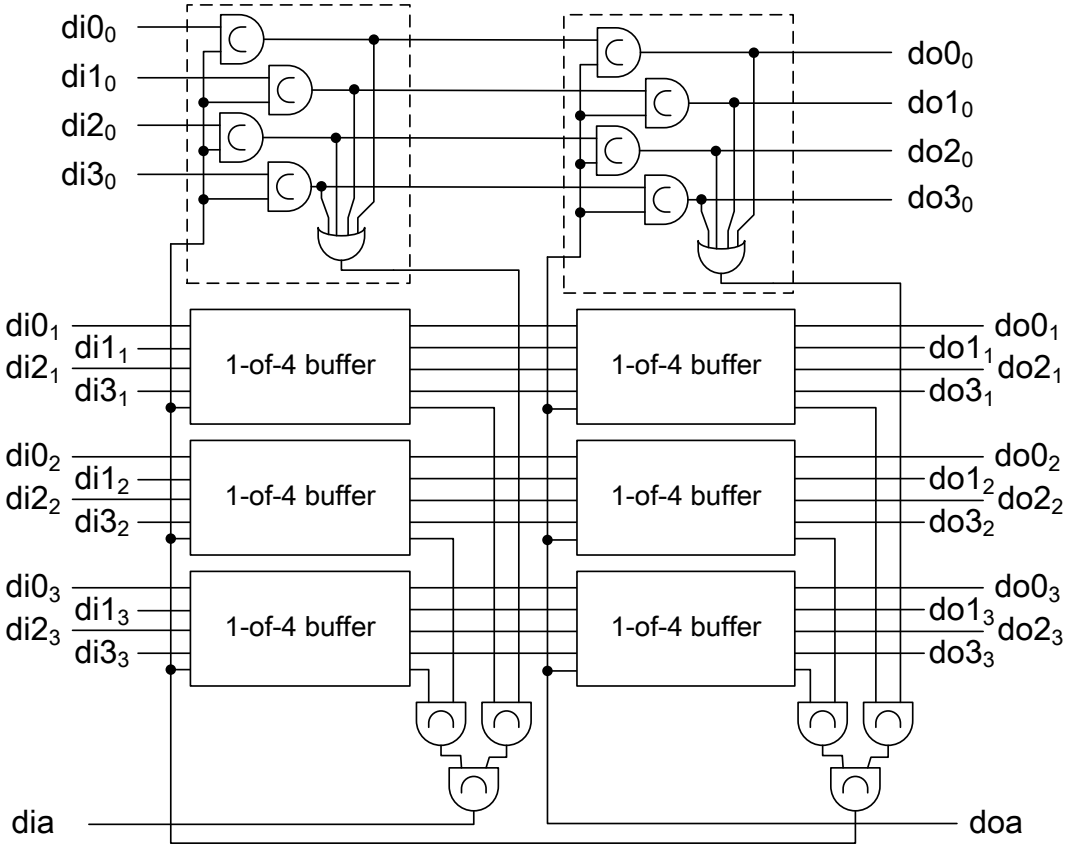
th_{SDM} (M=4)= 0.83

VC vs. SDM

- VC
  - Extra virtual channels (buffer)
  - An extra VC allocator
  - Increased crossbar
  - ANoC, QoS NoC, MANGO, QNoC
- SDM
  - Increased crossbar plus extra control logic
  - No asynchronous implementation

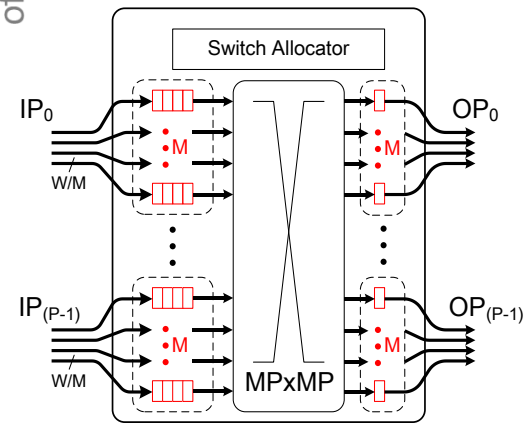
Input/Output Buffer

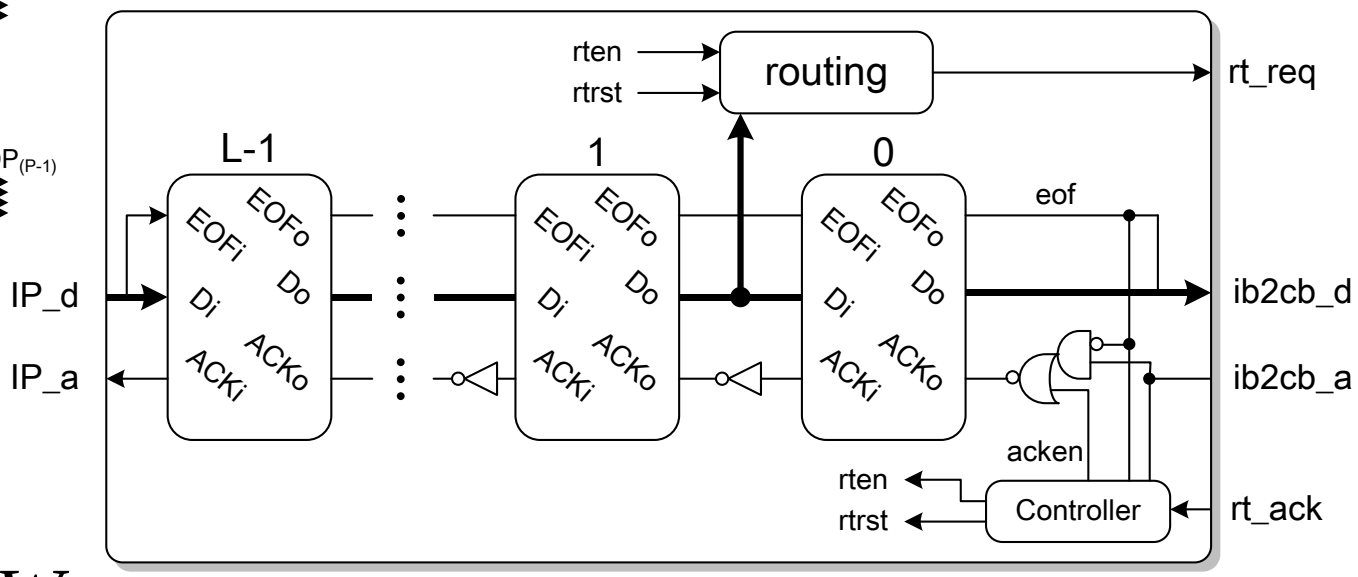




$$A = 2.5WA_C L$$

Input/Output Buffer

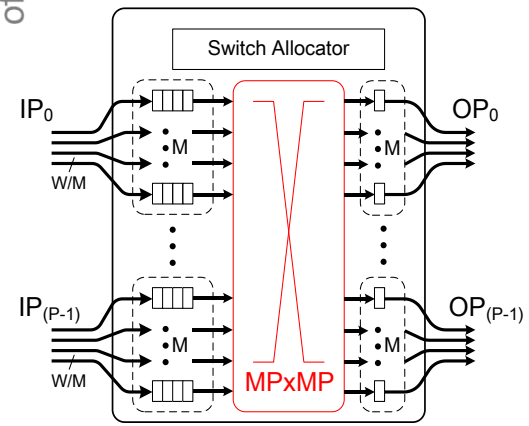


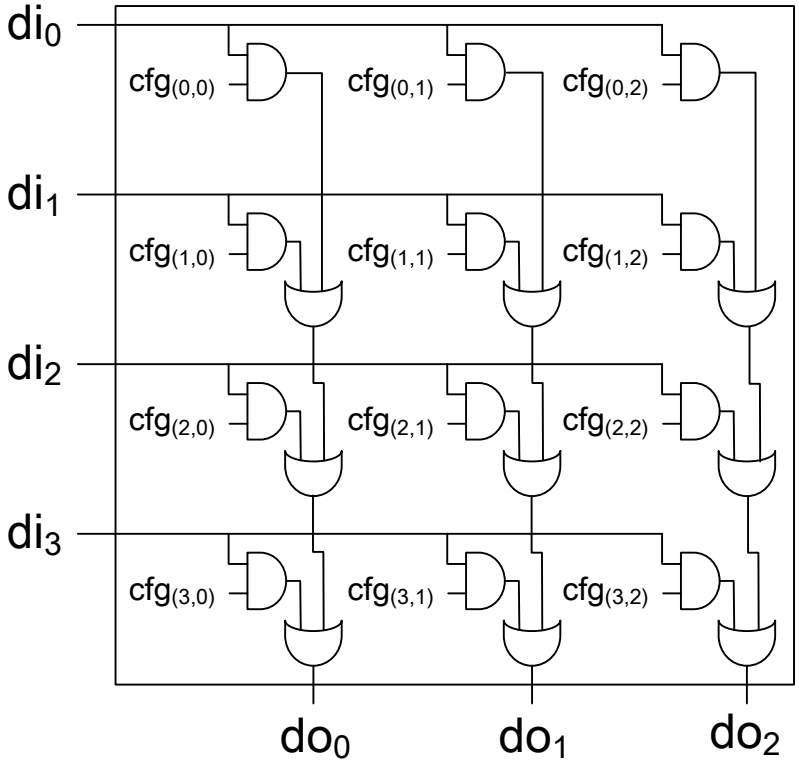


$$A_{IB} = M[L(2.5\frac{W}{M}A_C + A_{EOF}) + A_{RC} + A_{CTL}]$$

$$A_{OB} = 2.5WA_C + MA_{EOF}$$

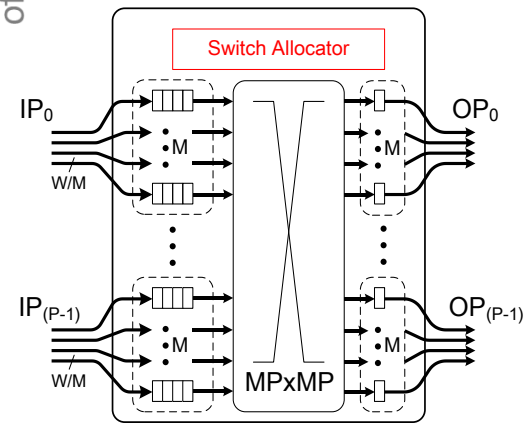
Crossbar

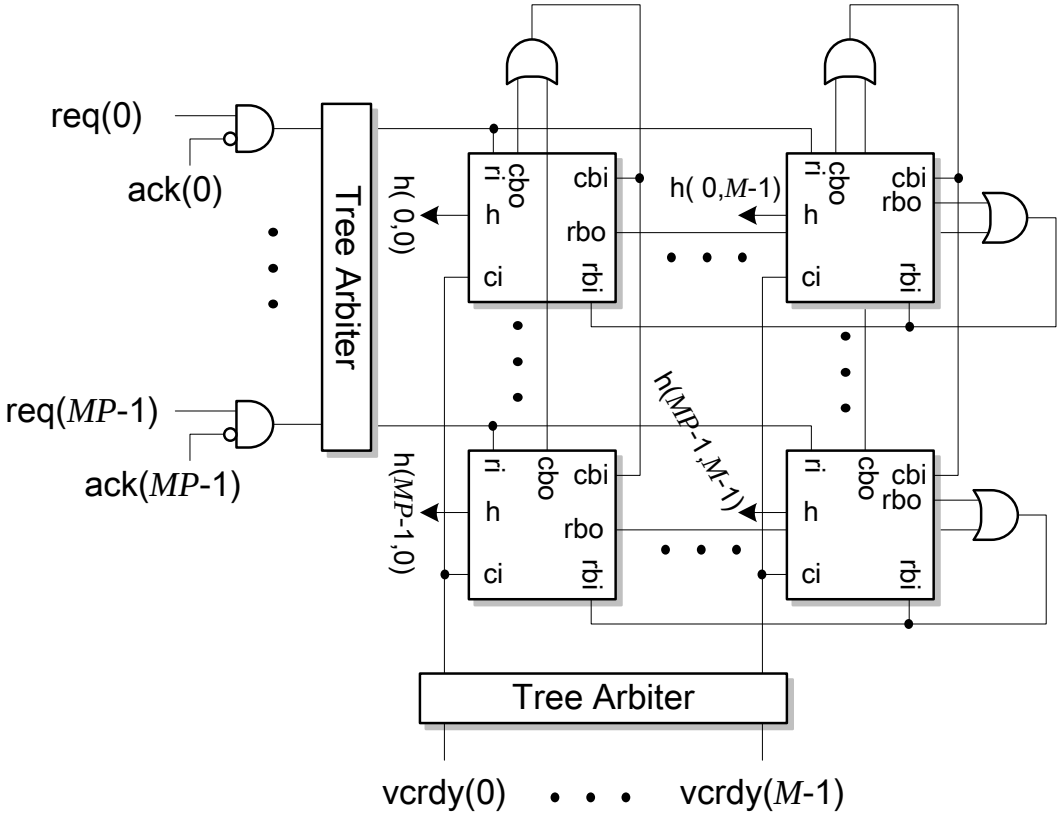




$$A_{CB} = (\frac{2W}{M} + 2)(2M^2P^2 - MP)A_g$$

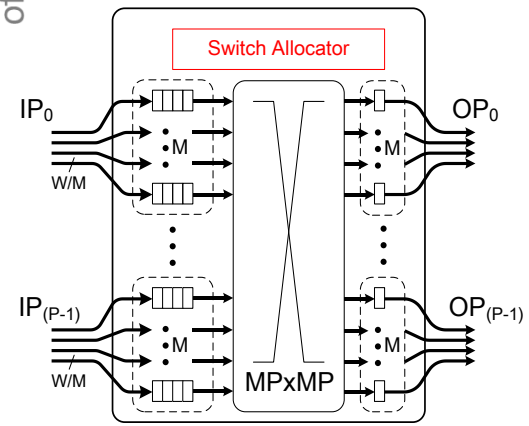
Switch Allocator

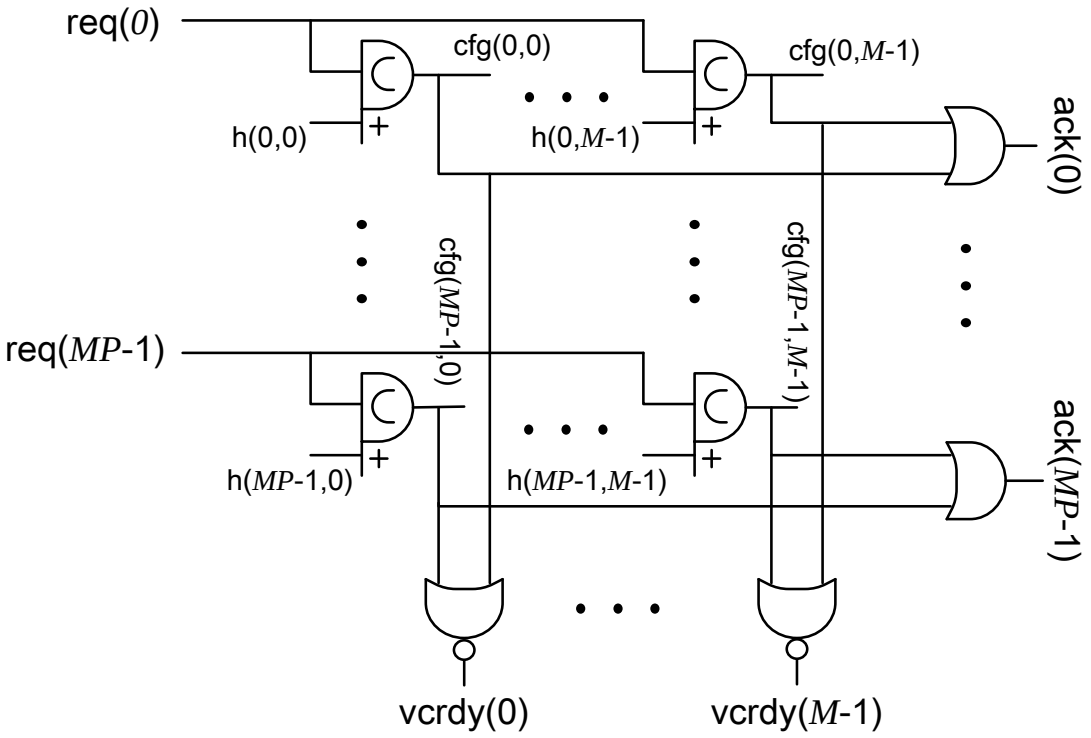




- S. Golubcovs, D. Shang, F. Xia, A. Mokhov, and A. Yakovlev, “Modular approach to multi-resource arbiter design,” ASYNC 2009.

Switch Allocator





$$A_A = M^2 P^2 A_{arb}$$

Area Consumption

- Wormhole

$$A_{IB,WH} = L(2.5WA_C + A_{EOF}) + A_{RC} + A_{CTL}$$

$$A_{OB,WH} = 2.5WA_C + A_{EOF}$$

$$A_{CB,WH} = (2W + 2)(2P^2 - P)A_g$$

$$A_{A,WH} = P^2 A_{arb}$$

- SDM

$$A_{IB,SDM} = M[L(2.5\frac{W}{M}A_C + A_{EOF}) + A_{RC} + A_{CTL}]$$

$$A_{OB,SDM} = 2.5WA_C + MA_{EOF}$$

$$A_{CB,SDM} = (\frac{2W}{M} + 2)(2M^2P^2 - MP)A_g$$

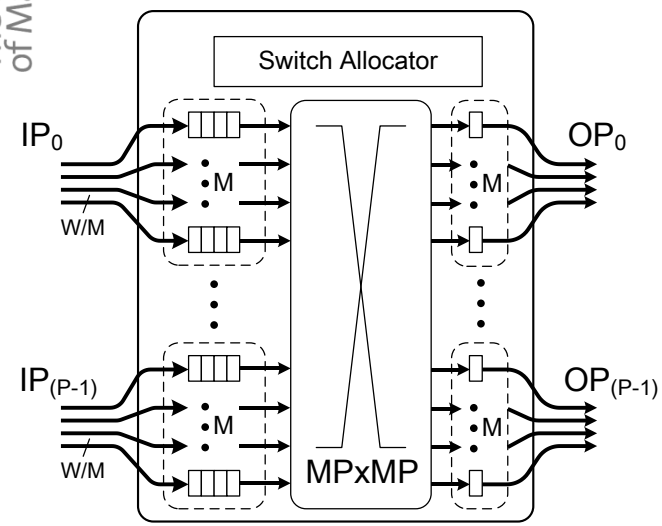
$$A_{A,SDM} = M^2P^2A_{arb}$$

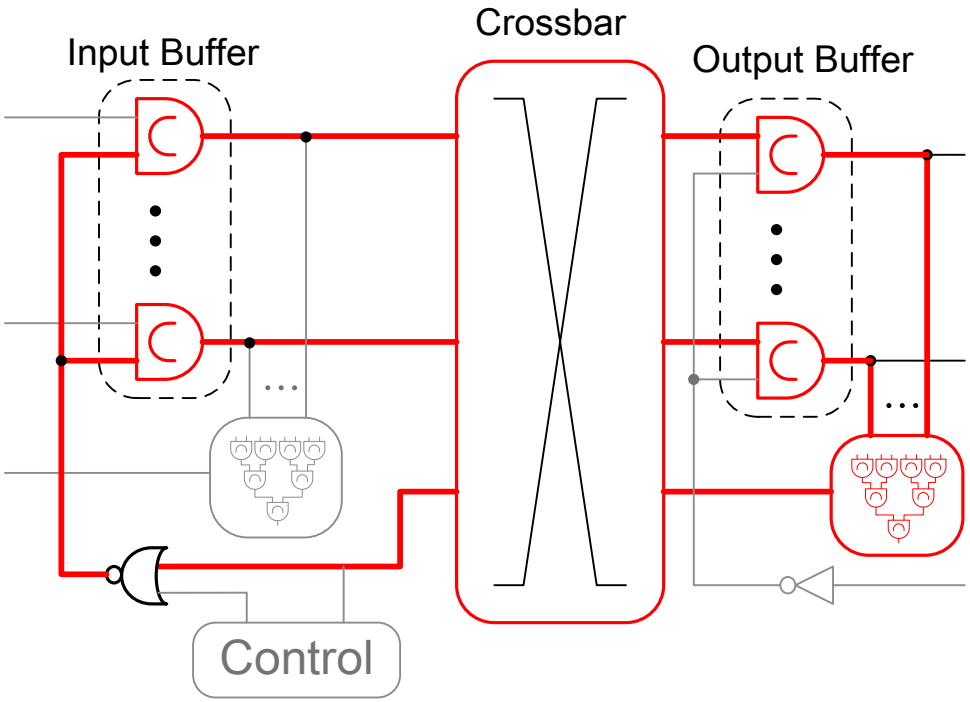
Area Consumption

	WH	err(%)	SDM	err(%)
Input Buffers	14,303	0.0	21,995	-0.4
Output Buffers	5,935	0.0	6,000	1.7
Crossbar	4,356	0.0	21,744	-0.2
Switch Allocator	772	78.2	22,208	-0.9
Total	25,366	2.4	71,956	-0.3

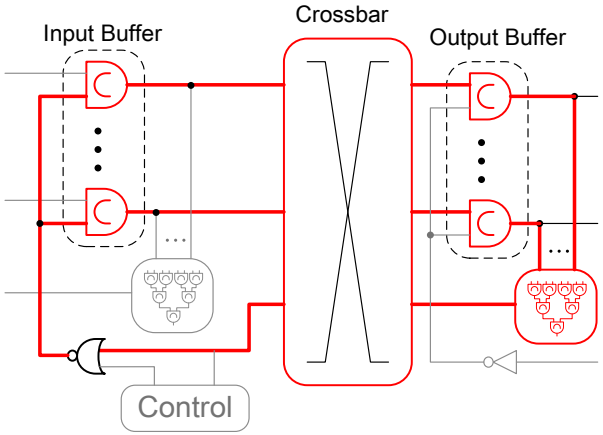
P=5, L=2, W=32, M=4

Critical Cycle





Critical Cycle



$$T = 4t_C + 4t_{CB} + 2t_{CD} + 2t_{AD} + t_{CTL}$$

$$t_C = \begin{cases} l_C + k_C(P+1) & wormhole, \\ l_C + k_C(MP+1) & SDM. \end{cases}$$

$$t_{CB} = \begin{cases} l_{CB} + k_{CB}\log_2(P) & wormhole, \\ l_{CB} + k_{CB}\log_2(MP) & SDM. \end{cases}$$

$$t_{AD} = \begin{cases} l_{AD} + k_{AD}(2W+1) & wormhole, \\ l_{AD} + k_{AD}(\frac{2W}{M}+1) & SDM. \end{cases}$$

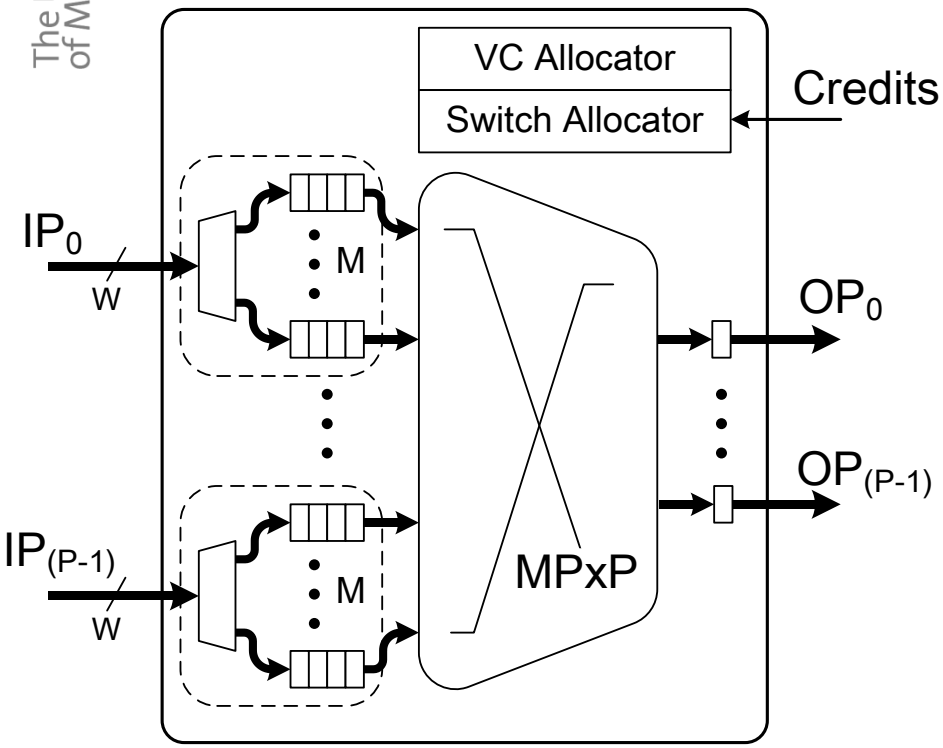
$$t_{CD} = \begin{cases} l_{CD} + l_C\log_2(\frac{W}{2}) + k_{CD}P & wormhole, \\ l_{CD} + l_C\log_2(\frac{W}{2M}) + k_{CD}MP & SDM. \end{cases}$$

Critical Cycle

	WH	err	SDM	err(%)
cycle period	4.25	2.6	4.15	-3.4
router latency	2.29		2.49	
routing calculation	0.44		0.51	
switch allocation	0.78		3.21	
t_C	0.22	-9.1	0.34	-5.9
t_{CB}	0.16	1.3	0.26	-3.8
t_{CD}	0.79	7.6	0.57	4.2
t_{AD}	0.57	6.1	0.27	-0.4

P=5, L=2, W=32, M=4

VC Router



$$A_{IB,VC} = MA_{IB,WH} \approx MA_{IB,SDM}$$

$$A_{OB,VC} = A_{OB,WH} \approx A_{OB,SDM}$$

$$A_{CB,VC} = (2MP^2 - P)(2W + 2)A_g \approx A_{CB,SDM}$$

$$A_{A,VC} = (M^2P^2 + MP)Aarb \approx A_{A,WH} + A_{A,SDM}$$

VC Router

$$t_{C,VC} = t_{C,WH} < t_{C,SDM}$$

$$t_{CD,VC} = l_{CD} + l_C \log_2(W/2) + k_{CD}MP > t_{CD,WH} > t_{CD,SDM}$$

$$t_{AD,VC} = t_{AD,WH} > t_{AD,SDM}$$

$$t_{CB,VC} = t_{CB,WH} < t_{CB,SDM}$$

cycle period = 5.23 ns

routing calculation = 0.44 ns

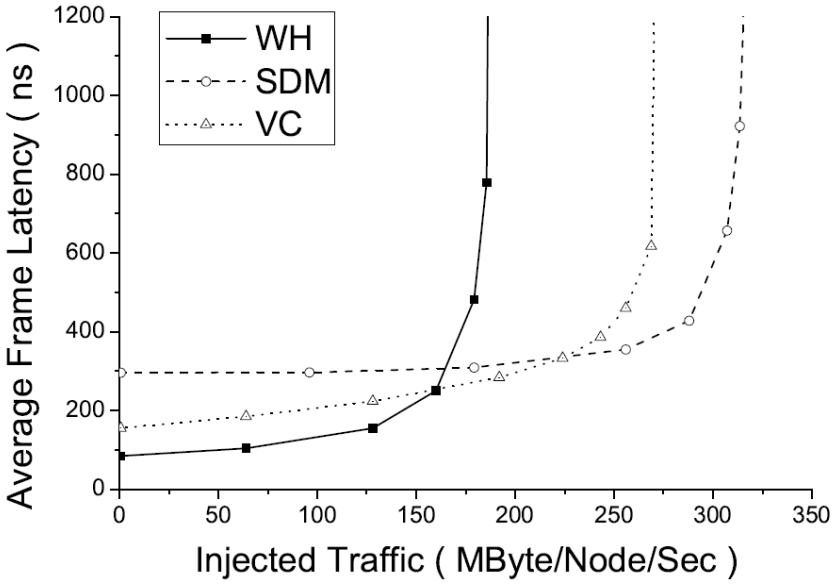
VC allocation = 3.21 ns

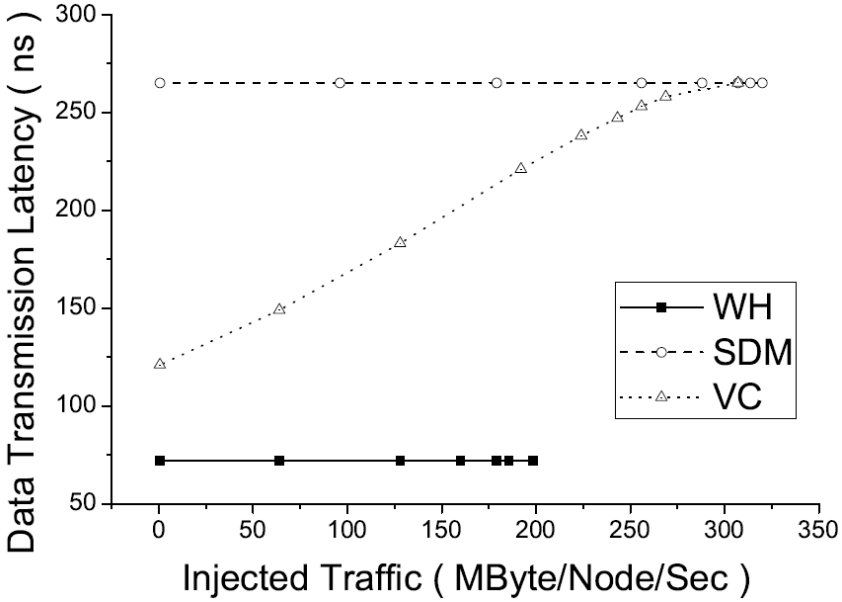
switch allocation = 0.78 ns

SystemC model

- Latency accurate SystemC models
- Wormhole, SDM, VC
- 8x8, 5 ports, XY routing
- 32-bit, 4 VCs/virtual circuits

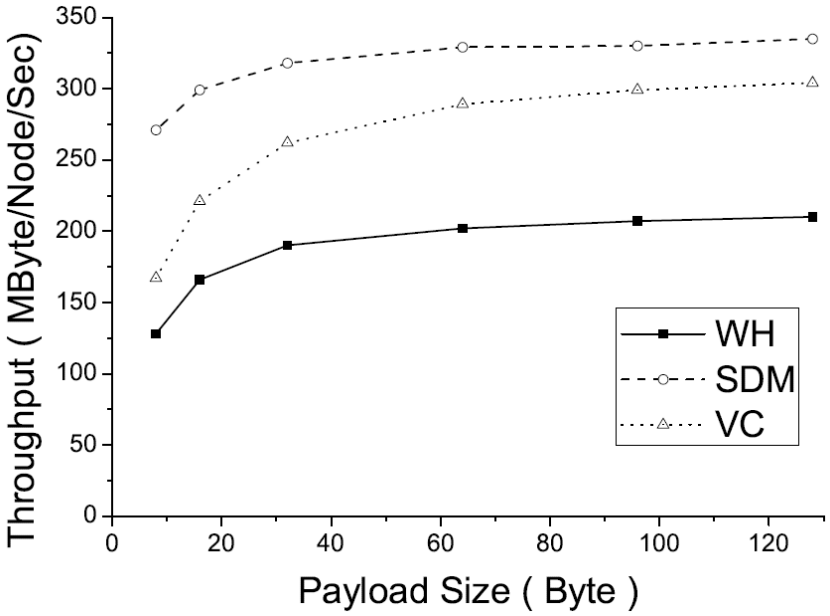
Average Frame Latency

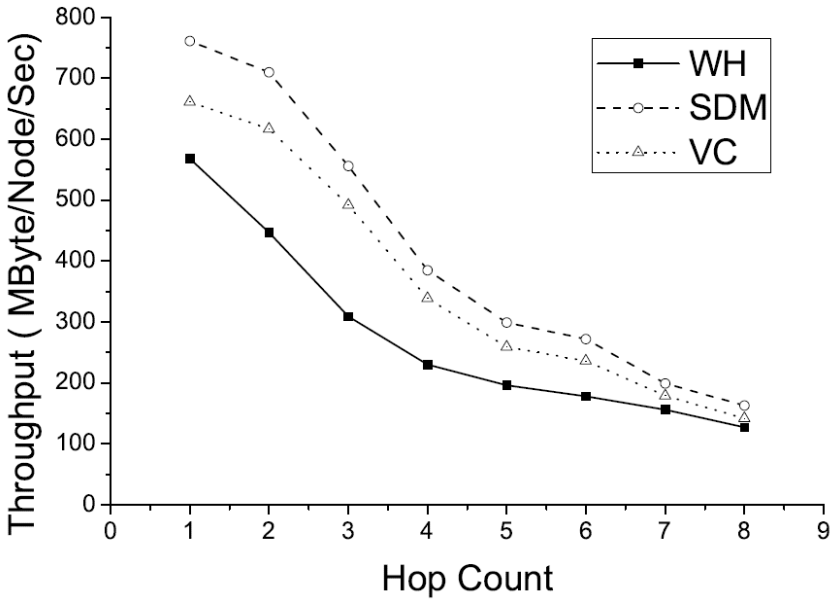




L=2, W=32, FL=64
VC router with L=2 suffers from credit loop stall.
Both SDM and SDMCS outperform VC.
Wormhole, SDM and SDMCS have constant data transmission latency.

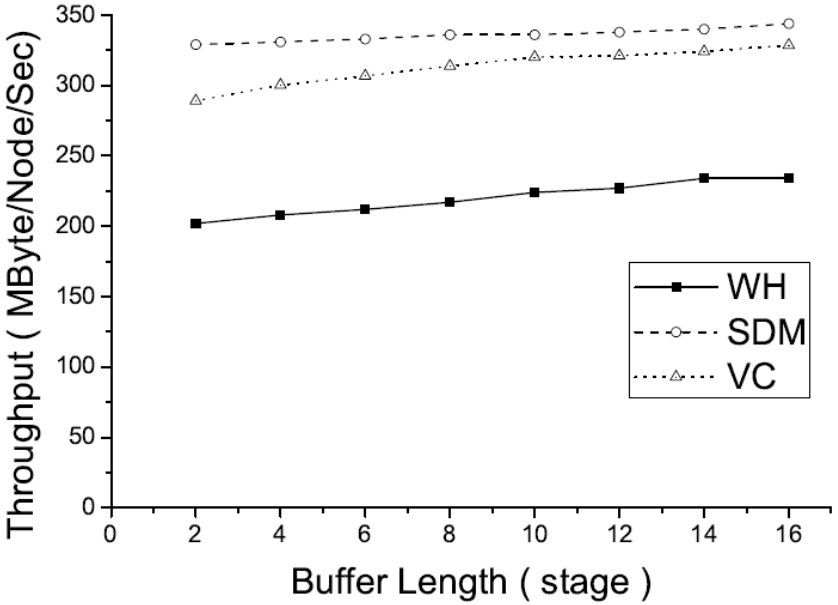
Payload Size and Distance

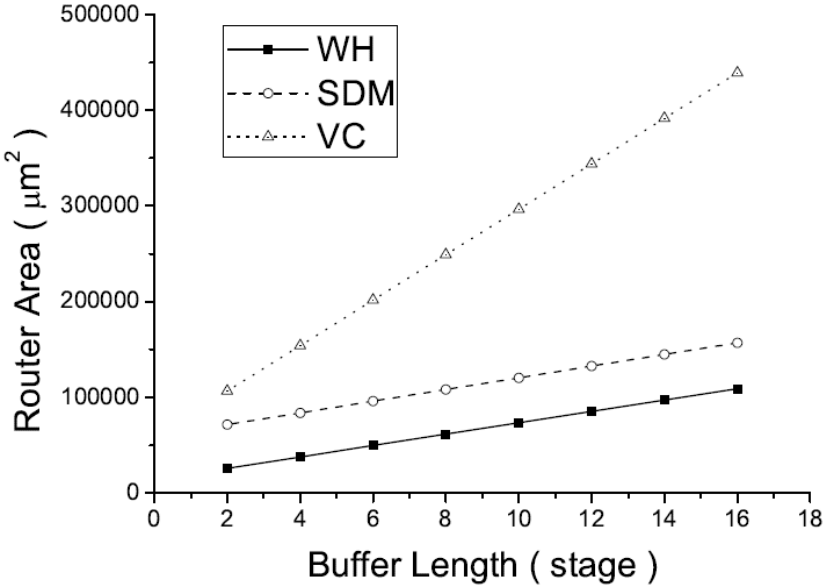




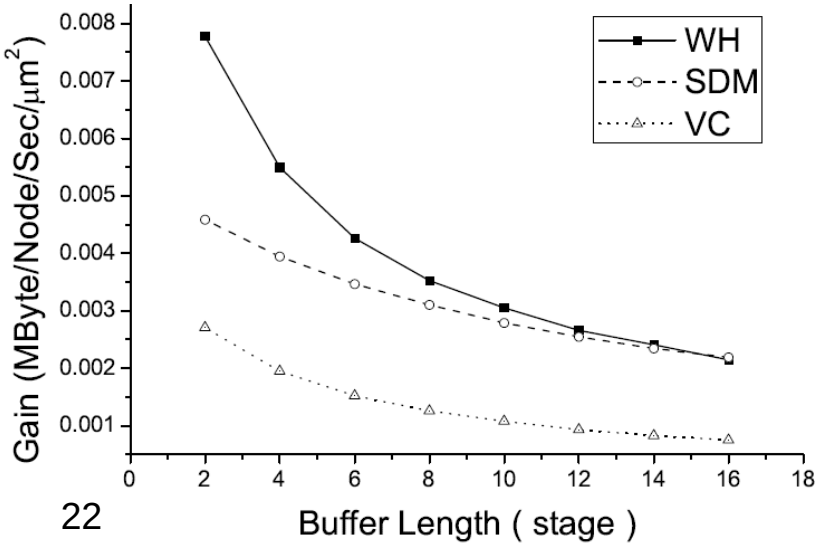
All routers approach the maximal throughput with longer payload length.
FL=64 Byte shows 90% maximal throughput.
Throughput decreases with the increasing hop count.
SDM shows better through even in the 8-hop case

Buffer Size





$$Gain = \frac{throughput}{area}$$



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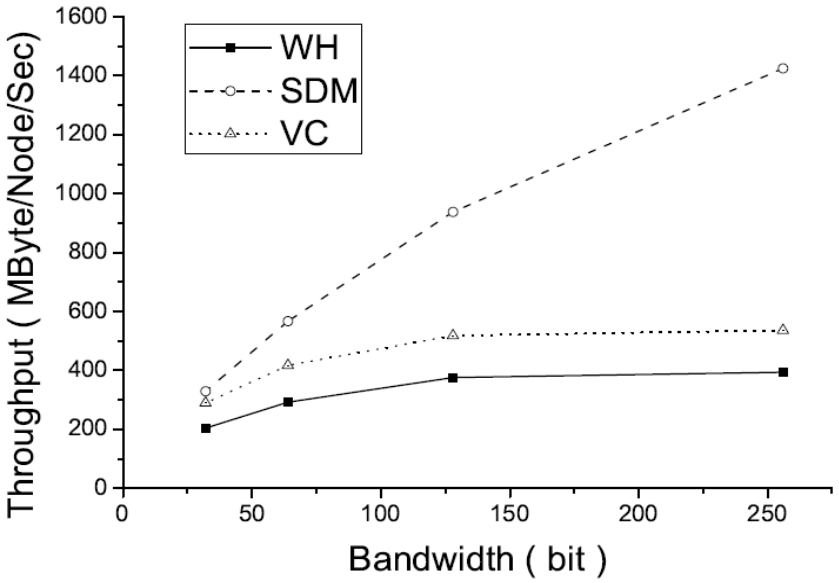
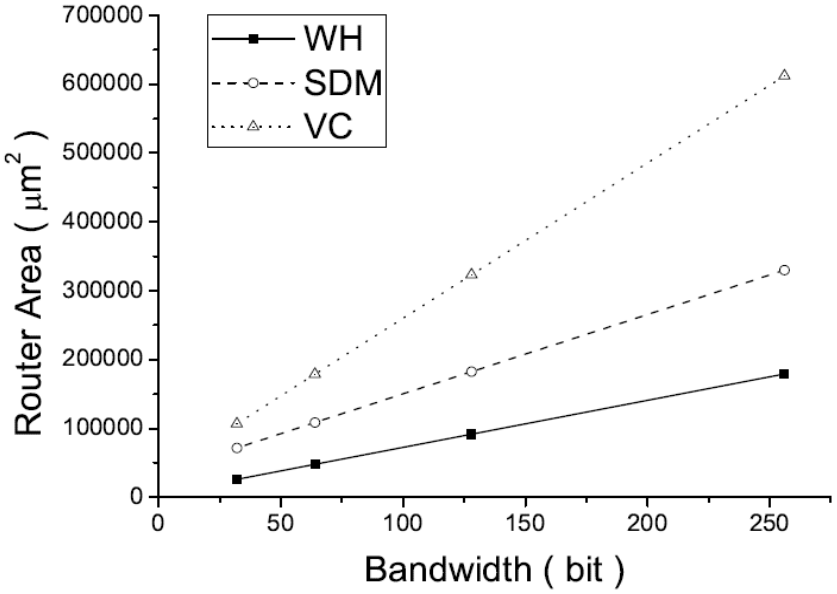
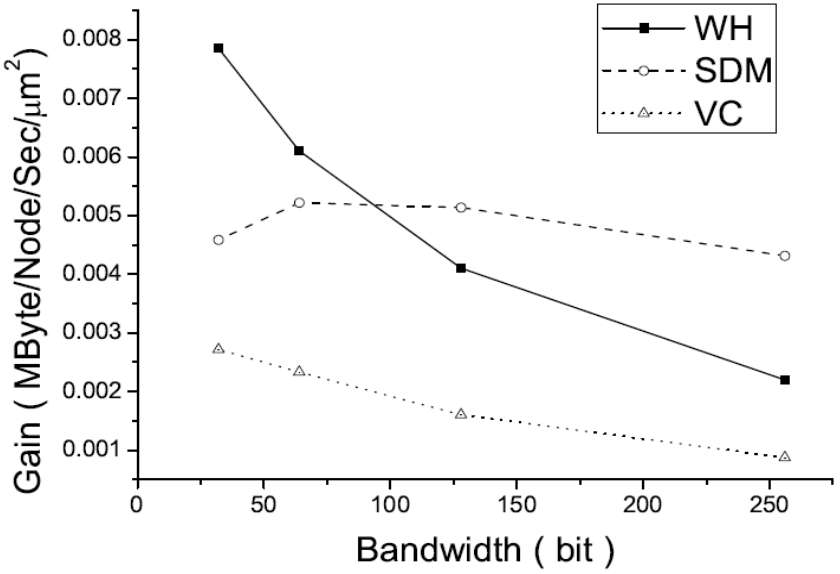
Data Width





$$Gain = \frac{throughput}{area}$$



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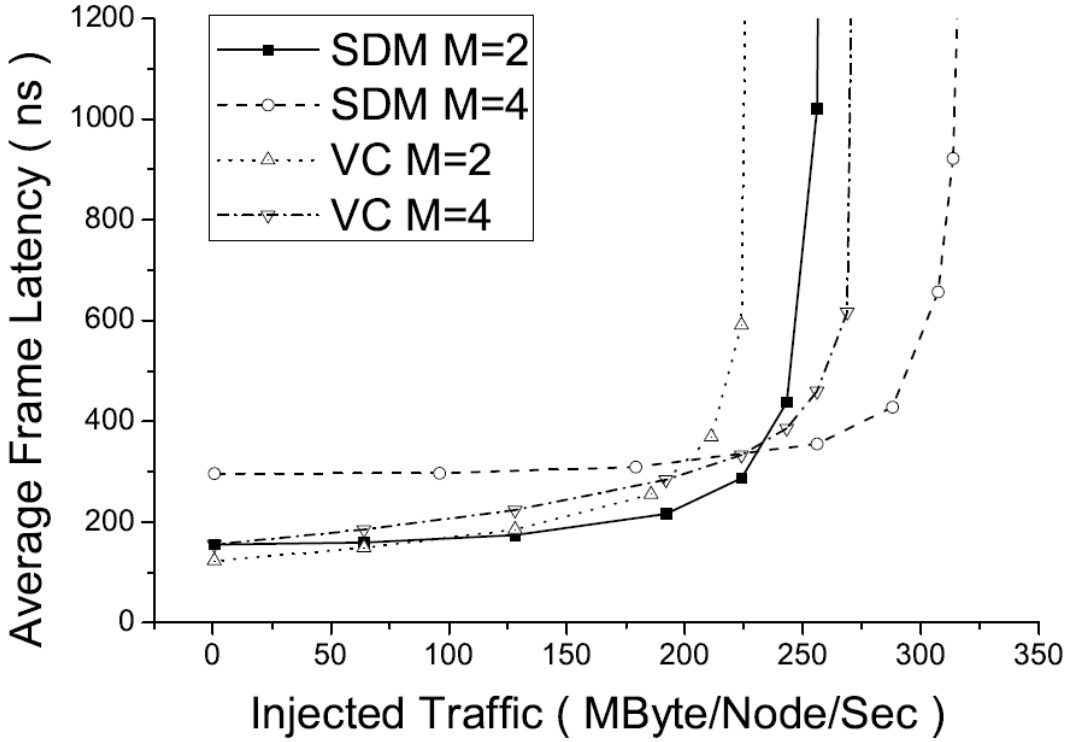
Number of VCs



Conclusions

- Both VC and SDM improve throughput.
- SDM achieves better throughput performance and area to throughput gain than VC.
- SDM has the potential ability to support hard delay guaranteed services

Thanks!

Question?