# ASYNCHRONOUS ON-CHIP NETWORKS AND FAULT-TOLERANT TECHNIQUES

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*To Chunzhen and Chao for their patience and love.*
*To Mingyi and Jersey for bringing joy into our life.*

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# Contents

# Preface

We have entered an era of multicore processors as the single-core performance has reached its ceiling along with the slowing down of the Moore's Law. Current mainstream commercial processors, such as Intel Core and Xeon, and AMD Ryzen and Epyc, are all multicore processors which contain up to 64 processing cores. In the foreseeable future, the number of cores in a processor will continue to increase.

When the number of cores reaches tens to hundreds, a significant portion of the total design effort would be dedicated to making the core-to-core communication speed and energy efficient. Although currently almost all processors use synchronous on-chip networks built by synchronous circuits, asynchronous on-chip networks may become useful or even necessary in the near future. In synchronous on-chip networks, the global clock needs to be distributed over long distances with little clock skew, which becomes a challenge as the network scales. It is estimated that the clock tree could consume 20% to 50% of the total power in synchronous circuits while the synchronous on-chip network could consume 33% to 36% of total power. To reduce the total power consumption, it is common to let individual processing cores implemented in their own clock and power domains, and run at their own clock frequencies dynamically tuned according to real-time work load. In this scenario, an asynchronous on-chip network might be a better candidate than a synchronous one.

This is a book about how to design a high throughput and fault-tolerant asynchronous on-chip network for multicore and many-core processors. The state-of-the-art way of designing and optimizing asynchronous on-chip networks is to mimic the structure of synchronous on-chip networks. However, the timing division multiplexing (TDM) techniques extensively utilized in synchronous

networks introduce extra synchronization and largely increase the speed penalty in asynchronous on-chip networks. Instead of TDM, we would like to introduce spatial parallelism into asynchronous networks to improve their throughput performance without incurring the synchronization penalties.

There is one annoying problem with the asynchronous on-chip networks built by quasi-delay-insensitive (QDI) circuits: They are sensitive to faults. A fault does not only corrupt a data packet, it also obstructs the handshake protocol essentially needed for correct data transmission, disrupts the normal data flow and may finally produce a deadlock paralyzing the whole network. The second half of this book is dedicated to this issue. A fault-tolerant coding method is proposed to tolerate transient faults. When a deadlock is caused by a fault, the location of the fault is first accurately pinpointed using a fault detection circuit and the network is then functionally resumed by isolating the faulty components.

This book is intended for researchers, engineers and students who research QDI and speed-independent (SI) circuits, asynchronous on-chip networks and switching networks built on QDI and SI circuits, fault-tolerant QDI circuits and finally the fault-tolerant asynchronous on-chip networks.

The organization of the book follows a self-contained manner. Chapters are carefully ordered in a way that necessary background knowledge and related topics are introduced and discussed before an advanced technique is described. Readers can read through the book without resorting to related research papers and books, but they are provided in the bibliography for further references.

*Introduction* provides a context for the topics described in this book, including our motivation in doing these researches, their applications in current and future computer systems and the state of the art in related areas.

*Asynchronous Circuits* introduces the concept of asynchronous circuits, the timing assumptions used in different types of asynchronous circuits and the implementation of asynchronous circuits.

*Asynchronous Networks-on-Chip* describes all the general concepts of on-chip interconnects necessary for understanding this book. This chapter also introduces asynchronous on-chip networks.

*Optimizing Asynchronous On-Chip Networks* improves the throughput performance of asynchronous on-chip networks by introducing spatial parallelism into the router design.

*Fault-Tolerant Asynchronous Circuits* begins to analyze the effect of faults on asynchronous circuits, and presents the state-of-art fault-tolerant techniques for asynchronous circuits. It shows that faults not only corrupt data but can also bring down the whole asynchronous network.

*Fault-Tolerant Coding* introduces the fault-tolerant encoding for asynchronous circuits and proposes a fault-tolerance delay-insensitive redundant check code for QDI interconnections that can tolerate transient faults.

*Deadlock Detection* describes how to detect a deadlock caused by a fault on asynchronous on-chip networks and how to locate the faulty link. This is the prerequisite for a network to recover from a fault-caused deadlock.

*Deadlock Recovery* presents deadlock recovery techniques, including an asynchronous router design and on-chip network design that can recover from a deadlock caused by faults.

*Summary* concludes the book and introduces the future work.

This book is based on our Ph.D. research work done in the Advanced Processor Technologies (APT) group in the School of Computer Science at the University of Manchester. We are greatly indebted to our supervisors, Dr. Doug Edwards and Dr. Jim Garside. They brought us into the world of asynchronous circuit designs, carefully guided us with their wide knowledge and insight and constantly encouraged us using their deep passion in research. We would like to express our gratitude also to the colleagues in the APT group for their direct and indirect help to this research.

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CHAPTER 1

# Introduction

The advancing semiconductor technology makes it possible to integrate more and more processing cores on a single chip to achieve continuously increasing chip performance, posing a growing demand for scalable and efficient interconnection. On-chip networks (OCNs) or Networks-on-Chip (NoCs) have emerged as a promising candidate to support large-scale on-chip communication. Most existing NoCs are built synchronously, which could be restricted by issues induced by the growing clock distribution as the network scales. As an alternative, event-driven asynchronous circuits which are controlled by handshake protocols rather than global clocks, can be employed to implement NoCs. Removing the clock, asynchronous NoCs have many attractive advantages over synchronous ones.

In the deep sub-micron era, reliability has become a challenge faced by the scaling electronics. Accompanied with the shrinking device dimensions, factors like the lowering voltage supply, the increasing clock frequency and the growing density of chips, have a negative impact on the chip reliability. Electronic systems are more susceptible to *faults*. *Fault tolerance* has become an essential objective for critical digital systems.

Fault tolerance has been systematically studied in traditional synchronous NoCs, but rarely in asynchronous ones. Using one timing-robust class of asynchronous circuits — the quasi-delay-insensitive (QDI) circuits — to implement the NoC, QDI NoCs can naturally tolerate delay variation, which is attractive for large-scale

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NoCs. Faults have more complicated and devastated impact on QDI NoCs compared with synchronous NoCs, which is a challenging issue needed to be resolved. This book talks about the fault-tolerant on-chip networks implemented by asynchronous circuits, and targets providing holistic, efficient, resilient and cost-effective fault-tolerant solutions to asynchronous NoCs.

## 1.1 ASYNCHRONOUS CIRCUITS

Asynchronous circuits work in a clockless and self-timed manner. They are designed under certain timing assumptions, which describe their tolerance to the delay variance of gates and wires. This book concentrates on one specific timing-robust type of asynchronous circuits, the quasi-delay-insensitive (QDI) circuit, which tolerates arbitrary positive delay on all gates and wires except for some forks that are assumed isochronic (wires that have equal latency to all its fanouts). Since its strong tolerance to delay variation, QDI circuit remains functioning under extreme working conditions, such as sub-threshold supply voltage and ultra low/high temperature, naturally tolerates process variation which becomes increasingly troublesome for synchronous circuits, and requires less static timing analysis than all other types of asynchronous circuits, not to mention the synchronous ones. In addition, QDI circuit is presumably low power because it wastes no power on the clock tree and consumes nearly zero power when it is not actively in use.

Although asynchronous circuits have a long history of over 50 years [163], most very large-scale integration (VLSI) circuits are synchronous due to the mature electronic design automation (EDA) support. Since registers and latches in synchronous circuits are synchronized by the global clock, they are the natural timing boundaries by which a circuit can be divided into paths. All these paths are driven by the same clock and operate concurrently and independently. EDA tools, especially synthesis tools, are therefore able to improve speed by optimizing these paths individually. On the other hand, the latches in asynchronous circuits are driven by handshake protocols (circuits). The operation of one latch is normally triggered by events generated from other latches. It is difficult to optimize the speed of asynchronous circuits due to the lack of clear timing

boundaries to break large circuits into small analyzable pieces as in synchronous circuits. Some asynchronous synthesis tools have been proposed recently, such as Petrify [57] and Balsa [73], to translate behavioral hardware descriptions into low level netlists. However, high-speed asynchronous circuits are almost always manually designed [182, 212, 219].

Shrinking transistor geometry brings opportunities for asynchronous circuits. As the number of transistors in a single die increases corresponding to the prediction of Moore's Law, the area and power overhead of synchronizing the whole chip with one global clock is unacceptable and beyond the control of current EDA tools. Future multicore processors should be globally asynchronous and locally synchronous (GALS) designs where synchronous intellectual property (IP) blocks talk with each other using an asynchronous communication infrastructure. 49% of the global signals will be driven by asynchronous circuits by the year 2024 [104]. Variation is another problem. The decreasing transistor size increases power density which leads to temperature and power variations [98]. Process variation worsens the situation with non-deterministic cell latency. The worst case timing analysis in synchronous circuits generates over-pessimistic speed estimation [31]. Asynchronous circuits are tolerant to variations and provide average speed performance.

Designing asynchronous circuits is not an easy task compared with their synchronous counterparts. Without the mature support of commercial EDA tools, asynchronous circuits are usually fully or partially manually crafted. For this reason, this book demonstrates how to design QDI circuits from scratch by describing all implementations in gate-level Verilog HDL using normal gates available in any standard cell libraries.

## 1.2 ASYNCHRONOUS ON-CHIP NETWORKS

Current multicore processors use on-chip networks as their communication fabric. Most networks-on-chip (NoCs) are synchronous networks where network components are driven by the same or several global clocks. Thanks to the timing assumptions allowed by the global clock and mature EDA tools, these synchronous NoCs are

fast and area efficient. However, there are several design challenges in synchronous NoCs that are difficult to resolve:

- *Support for heterogeneous networks*: Unlike chip multiprocessor (CMP) systems where every network node is a homogeneous processor element, a multiprocessor system-on-a-chip (MPSoC) is a heterogeneous system where network nodes are IP blocks with different functions and hardware structures. These IP blocks are provided and tested with different clock frequencies, area sizes and even working voltages. These differences complicate the network topology, compromise the latency performance of synchronous networks and make chip timing closure difficult to reach.

- *Low power consumption*: It is crucial to reduce the power consumption of an SoC as it determines the maximum standby time of a device. The clock tree of synchronous on-chip networks consumes a significant amount of energy [153], and it is getting worse along with the shrinking transistor geometry.

- *Tolerance to variation*: Process, temperature and voltage variations affect future sub-micron VLSI designs significantly [133, 138]. According to the international technology roadmap for semiconductors, the delay uncertainty caused by variations in the sign-off timing closure will reach 32% in 2024 [104]. Traditional static timing analysis is going to be replaced with statistical timing analysis methods [31] to cope with the dropping yield rate and the over-conservative timing estimation. Synchronous on-chip networks alleviate this effect by considering variations in their task mapping procedure [138]. However, this works only in homogeneous networks and the routers are still working at the worst estimated speed.

Instead of using synchronous on-chip networks, asynchronous on-chip networks are a promising solution to the above challenges. The communication components in an asynchronous on-chip network are built with clockless asynchronous circuits. Data are transmitted according to certain handshake protocols largely insensitive

to delay variations [231]. Because of this delay insensitivity, the interface between all IP blocks to the global asynchronous on-chip network is unified by the same synchronous to/from asynchronous interface. The fact that all synchronous blocks are isolated by the asynchronous network simplifies chip-level timing closure. Also, thanks to the delay insensitivity, an asynchronous on-chip network is naturally tolerant to all variations as the delay uncertainty caused by these variations cannot affect the function of those handshake protocols. Finally, since no clock is needed in asynchronous circuits, an asynchronous on-chip network consumes zero dynamic power when no data is in transmission.

However, asynchronous networks [11, 22, 28, 67, 75] are often slower than the synchronous on-chip networks with similar structures and resources [153]. Although the global clock in synchronous circuits is power consuming, it is a speed- and area-efficient approach to synchronize combinational operations. Asynchronous circuits rely on handshake protocols to control data transmission. Combinational operations are explicitly detected and guarded to ensure the insensitivity to delay. The circuits used in detecting combinational operations introduce area and speed overhead. Delay insensitive asynchronous circuits are intrinsically slow.

Another issue is that the state-of-the-art way of designing asynchronous on-chip networks is to asynchronously reproduce the structures of synchronous on-chip networks. As synchronous on-chip networks synchronize data with no speed penalty, timing division multiplexing (TDM) techniques [58] are extensively utilized. Simply reproducing such TDM structures in asynchronous on-chip networks introduces extra completion detection circuits and causes speed penalties.

Although the speed penalty of completion detection is unavoidable, as the promising advantages of asynchronous circuits are derived from those delay insensitive handshake protocols, the scale of the synchronization in asynchronous circuits can be limited to small transmission units, such as a single pipeline. The speed penalty is therefore alleviated. The following question is how to build asynchronous networks with such limited synchronization.

This book introduces techniques to improve network throughput by employing spatial parallelism in asynchronous on-chip

networks at different levels. Channel slicing is a new pipeline structure that alleviates the speed penalty of synchronization by removing it in bit-level data pipelines. It is also possible to further improve speed using the lookahead pipeline style if the QDI timing assumption is slightly relaxed. Spatial division multiplexing (SDM) is a flow control method that improves network throughput by removing the synchronization between flits of different packets, which is required by TDM methods on the contrary. The main cost of using SDM is a significantly increased crossbar inside each router. To reduce this area overhead, the crossbar can be replaced with novel switch structures, such as a novel 2-stage Clos switch dynamically reconfigured by an asynchronous dispatching algorithm.

## 1.3 FAULT-TOLERANT ASYNCHRONOUS ON-CHIP NETWORKS

On one hand, the advancing semiconductor technology boosts the chip performance and permits more processing cores to be integrated. On the other hand, accompanied with the shrinking device dimensions, all of the factors like the lowering power voltage, the increasing clock frequency and the growing density of chip impose a negative impact on the chip reliability [37].

In the deep sub-micron era, variations in manufacturing and operating conditions have a proportionately greater effect than before. Shrinking transistor dimensions means that variations in the actual manufacturing, such as dopant levels and crystal boundaries, influence transistor and wire properties with time [37]. Growing chip density results in a high heat flux across the die, creates hot spots with a high temperature, which affects the circuit performance and accelerates the device aging process. Reducing supplying voltage gives greater susceptibility to various noise sources [37, 56]. Increasing clock frequency raises the probability that noise creates faults on circuits. As a result, the sensitivity of electronic devices to environmental variations is significantly increased and the device aging process is accelerated.

It has been reported that the mean values of soft error rate (SER) of three circuits under a 40 *nm* process are 2.2E-4 FIT, 4.7E-4 FIT and 1.2E-4 FIT, respectively (1 FIT = 1 fail per 1 billion

hours) [257]. The 24 *MByte* of Level 3 Cache in an Intel Processor encountered 0.2∼2 errors per year under the SER of 0.0001∼0.001 FIT/bit [221]. An SER in the order of 0.001 FIT/bit has also been observed on the Altitude SEE test European platform [10]. It was predicted that the SER per logic state bit could increase 8% in each technology generation [95]. The SER in static random-access memory would increase 6∼7× from 130 *nm* to 22 *nm* process [102]. In 65 *nm* technology, the radiation can cause a 6.45× increase in SER when the supply voltage decreases from 1.0 $V$ to 0.33 $V$ [187]. It is believed that both the SER and the aging speed would increase as the technology continues scaling [37, 56, 84, 173]. Although researchers disagree on the absolute number of faults in particular circuits on particular processes, they all agree that the trend is for faults to increase as processes shrink. Electronic systems are more susceptible to *faults* [18], including *transient*, *intermittent* and *permanent* faults depending period of lasting [162]. The 2015 ITRS takes *reliability* as one main challenge faced by the next generation electronics and stresses the importance of a runtime protection [39]. Consequently, *fault tolerance* has become an essential design objective for critical digital systems, especially in highly specialized fields such as aerospace, military and medical equipment.

The fault tolerance of synchronous NoCs has been extensively studied. Faults typically cause data errors (or packet loss). These errors can normally be detected and corrected within several clock cycles. A clock signal provides a timing reference for error detection and correction. Detecting the error or packet loss, a retransmission can be requested to obtain the right packet [229]. However, there is no such timing reference in an asynchronous NoC. The QDI implementations are robust to timing variations but not to faults. A fault may pollute a transmitting packet, corrupt the handshake protocol and disrupt the normal data flow, which is a new challenge faced by asynchronous circuit designers. A single fault could even break the handshake protocol and results in a *fault-caused physical-layer deadlock*. This deadlock is different from the well-known network layer one induced by the cyclic dependence of multiple competing packets [61, 63]. Most conventional fault tolerant or deadlock management techniques for synchronous NoCs cannot work in a *deadlocked* state. The fault tolerance of asynchronous NoCs has

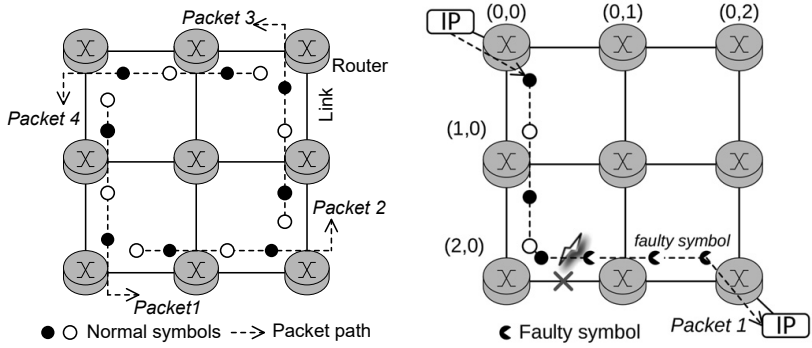
not been thoroughly studied. Various styles of asynchronous NoCs have been proposed but rarely do they have fault-tolerance capabilities [11, 30, 67, 75, 200, 212].

*Faults* can be classified into *transient*, *intermittent* and *permanent* faults depending on their duration [56]. Transient faults usually last for a short time and behave as positive or negative glitches (0→1→0 or 1→0→1) [18, 111]. Permanent faults will influence the victim gates or wires forever. Most permanent faults can be modeled as "stuck-at" faults [5, 137], where the logic level of a net is always 0 or 1. Intermittent faults usually happen as an early manifestation of permanent ones with the aging process [56]. They can appear as either transient or permanent during error detection or correction.

In the presence of faults, QDI NoCs behave differently from synchronous ones. A fundamental difference between synchronous and QDI circuits is the timing reference used in the transmission of data symbols.

- In synchronous circuits, a data symbol typically has a constant time per bit which can be agreed — and maintained for a known time — between the transmitter and the receiver. Corruption of the transmission will therefore affect a known number of bits. Thus faults on a synchronous NoC may corrupt packets being transmitted, lead packets to wrong destinations, result in packet loss or cause data errors. Nevertheless, the erroneous data symbol or faulty behavior can be easily detected and further corrected or recovered.

- There is no such timing reference in QDI circuits. Faults can insert or possibly delete symbols besides corrupting them. Managing these faulty cases represents a new challenge faced by QDI NoCs. Meanwhile, it is obvious that a permanent fault will stall the handshake and cause a physical-layer deadlock. Its detection and recovery has not been thoroughly studied in a NoC environment. More seriously, a transient fault cannot only cause data errors but also deadlock a QDI NoC, which has been neglected by the asynchronous community. These all increase the challenge of fault detection and recovery in QDI NoCs.




(a) Network-layer deadlock

(b) Fault-caused physical-layer deadlock

Figure 1.1 Network-layer and physical-layer deadlocks in a QDI NoC.

Deadlock is fatal to a NoC without any management mechanisms [61]. It can reduce the network performance, paralyze its function and eventually cause the chip to be discarded. The well-known *network-layer* deadlock due to the cyclic dependence of packets or restricted routings [63] can happen in all NoCs. Figure 1.1a shows an example where four packets hold and request network resources in a cyclic fashion, which is a network-layer deadlock. It can be resolved by using specific turn models or providing extra escape channels [63]. This network-layer deadlock is common in all NoCs and not the target of this book. In QDI NoCs, a fault may break the handshake protocol, resulting in a physical-layer deadlock, which is particular to QDI NoCs. Taking a simple (*req*, *ack*) handshake process for example, if the sender sends out a request to the receiver but without getting acknowledged, the sender does not know whether this is caused by a fault or delay because QDI circuit is insensitive to delay variations. It would keep waiting for the lost *ack*, resulting a physical-layer deadlock. Figure 1.1b illustrates a faulty case that a fault on a transmitting packet deadlocks the reserved data path in the network. Note that it is the adaptability of a QDI circuit to timing variations that makes it more vulnerable to this kind of deadlock-type faults. This

physical-layer deadlock cannot be easily resolved by higher-layer techniques for network-layer ones.

This book studies the impact of different faults on QDI NoCs, including transient and permanent ones, and proposes thorough and systematic fault-tolerant solutions to protect QDI NoCs. The achieved fault-tolerance capability and the incurred performance and hardware overhead are two main factors considered in the evaluation.

### 1.3.1 Protection for QDI Links

A large-scale NoC may contain a large number of long link wires, which are common in large-scale Systems-on-Chip (SoCs). Exposed to the external environment, they can be easily affected by various noise or fault sources and become the victim of timing variations or transient faults [14]. These chip-level long interconnects can be implemented as QDI pipelines to achieve high bandwidth and timing-robustness. However, a transient fault can be accepted as a valid signal in a QDI system, leading to the insertion, deletion or corruption of a data symbol. Fault-tolerant codes have been widely used to protect on-chip communication [229]. Codes also perform an important role in QDI circuits where delay-insensitive (DI) codes are used to build data symbols to encode the timing information. Most existing state-of-the-art fault-tolerant codes proposed for asynchronous circuits either compromise the timing-robustness of QDI circuits or incur large area and speed overhead. This book presents a novel delay-insensitive redundant coding (DIRC) scheme to protect QDI communication from transient faults, which can be easily adopted by existing DI or QDI interconnects without destroying their intrinsic timing-robustness. The protected QDI links can be constructed flexibly to satisfy various fault-tolerance requirement, with a moderate and reasonable hardware overhead.

### 1.3.2 Deadlock Detection

Both permanent and transient faults could break the handshake process in QDI NoCs and generate a physical-layer deadlock, which has more serious consequences to the system than pure data errors. The management of this fault-caused physical-layer deadlock

is significantly important to the chip life-span but it has barely been studied. To resume from a physical-layer deadlock, the network must go through two phases: deadlock *detection* and *recovery*. *Detection* of a fault-caused physical-layer deadlock is difficult in a QDI NoC. In a deadlocked state, error syndromes for fault analysis cannot be easily collected. Locating a specific defective wire or gate is difficult. The ideal situation is that the faulty component can be precisely located so that a recovery method can be further applied to bypass or replace the faulty component, which consequently resumes the network functionality. Therefore, an efficient and flexible detection method is necessary. It should be able to not only precisely locate the fault in the QDI NoC, but also differentiate the fault-caused physical-layer deadlock from other similar network scenarios, including the upper network-layer deadlock and the network congestion. When both transient and permanent faults are considered, an accurate model is needed to differentiate deadlocks caused by different faults, so as to enable the *fault diagnosis*. The proposed techniques should be able to detect, diagnose and locate the fault as long as the fault deadlocks the network.

### 1.3.3 Network Recovery

As the fault position has been located, the next step is to recover the network function according to the deadlocked state of the handshake protocol and the network protocol. Figure 1.1b shows one possible deadlock case where a fault deadlocks a reserved long packet path composed of the faulty link and other healthy network sources. A direct system reboot can temporarily remove this deadlock, but it is expensive and cannot deal with the deadlock caused by permanent faults. Therefore, a fine-grained recovery strategy is necessary to remove the deadlock and isolate the faulty component. The recovery contains two main processes: (1) deadlock removal, which recovers the stalled packet flow in the deadlocked packet path, releasing blocked healthy network resources and eliminating the deadlock and (2) faulty link isolation: instead of using upper network-layer methods such as fault-tolerant routings to detour the faulty link, this book proposes a fine-grained recovery technique at the lower physical layer to isolate the faulty component and restore

the network function. Upper layer recovery techniques can further be used to improve the network performance after the loss of the faulty component. When transient and intermittent faults deadlock the network, the isolated link should be resumed when the fault fades.

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