

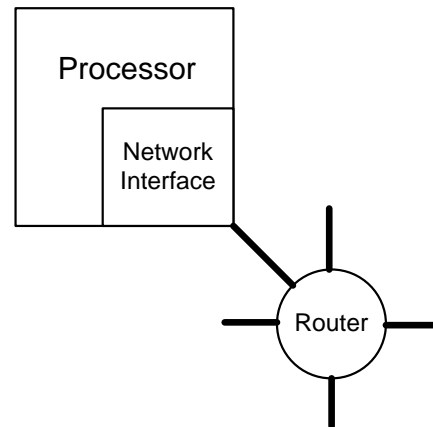
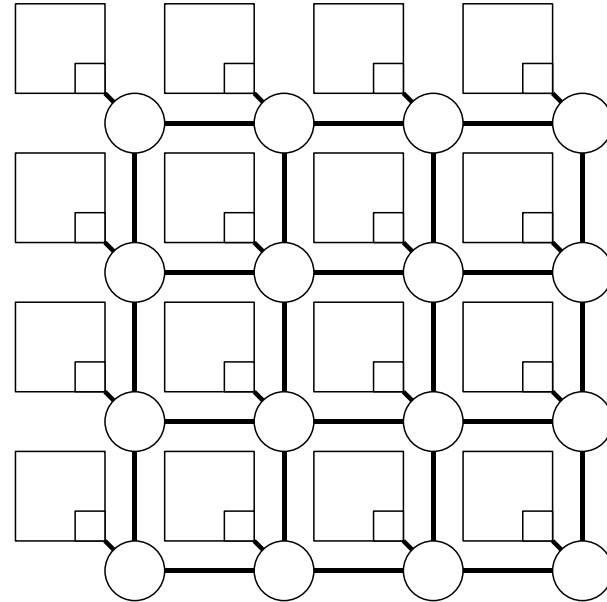
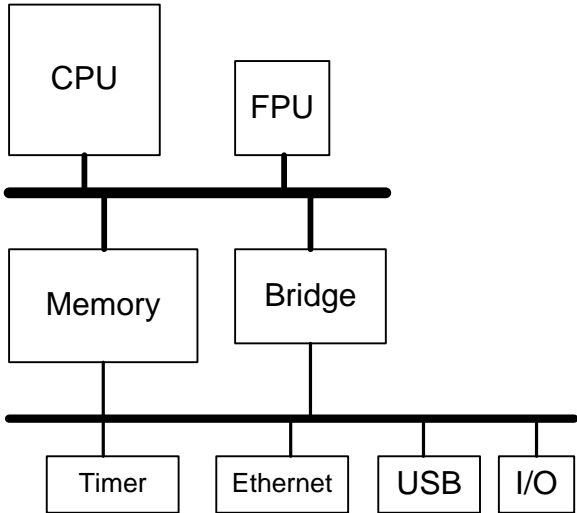
# From Channel Slicing to Spatial Division Multiplex for Asynchronous Networks-on-Chip

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Advisor: Christopher Harrison

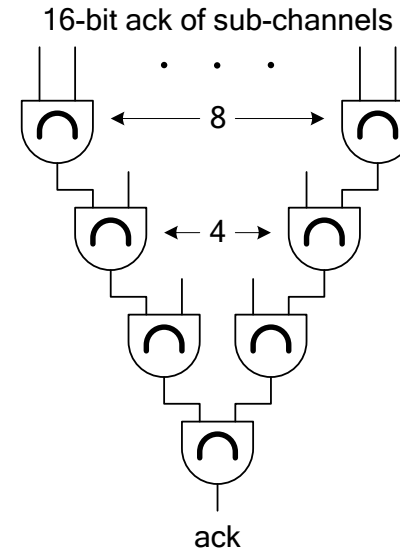
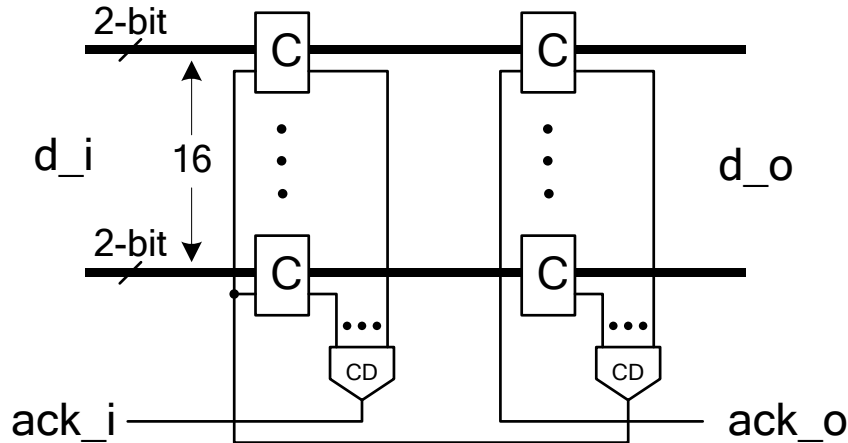
# Background: Networks-on-Chip



# Synchronous/Asynchronous

- Synchronous
  - Clock triggered
  - Fast
  - Small
  - Power Consuming
  - Sensitive to variation
  - Complex clock tree
- Asynchronous
  - Handshake
  - Slow !!
  - Large
  - Power Efficient
  - Tolerance to variation
  - No clock tree

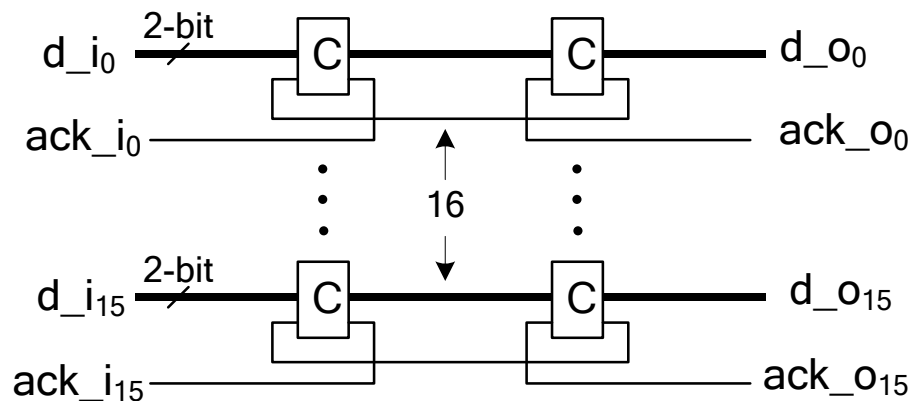
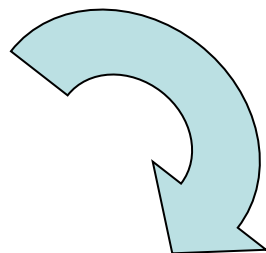
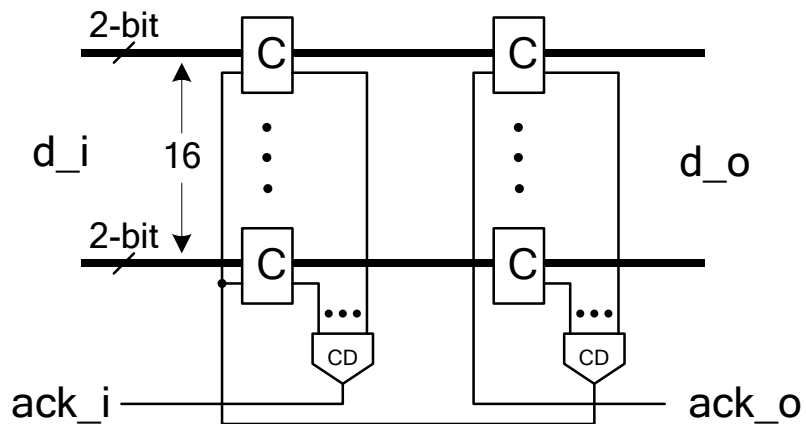
# Why asynchronous is slow?



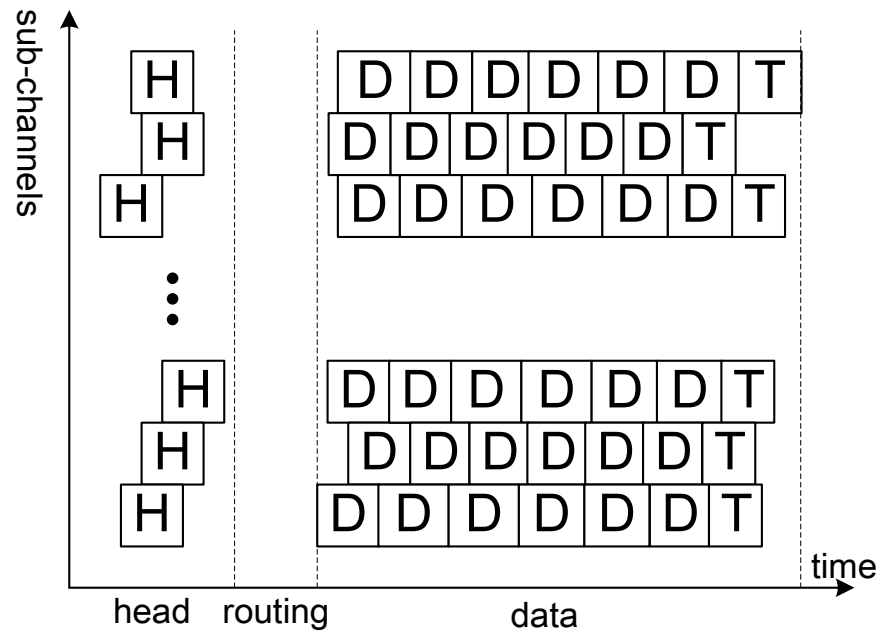
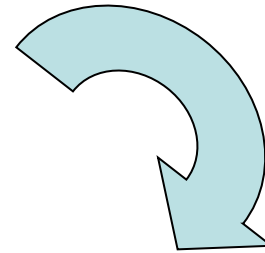
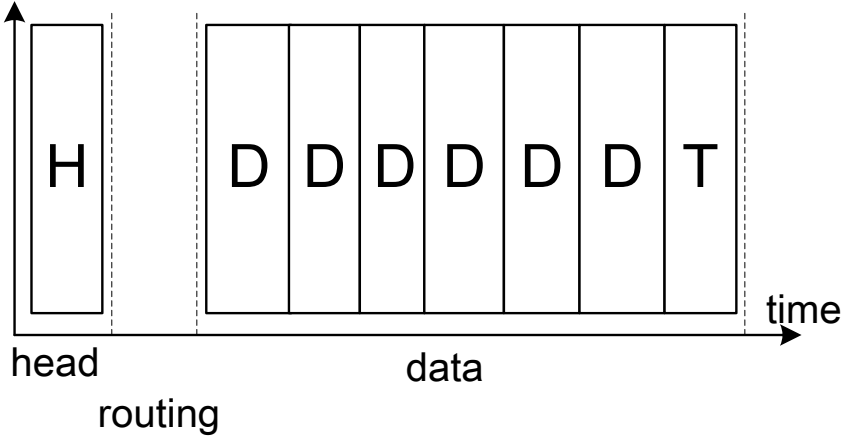
Advantages: data on all sub-channels are synchronized, ease the time division multiple access (TDMA) techniques, such as virtual channel and TDMA

Drawbacks: low speed (66% on CD)

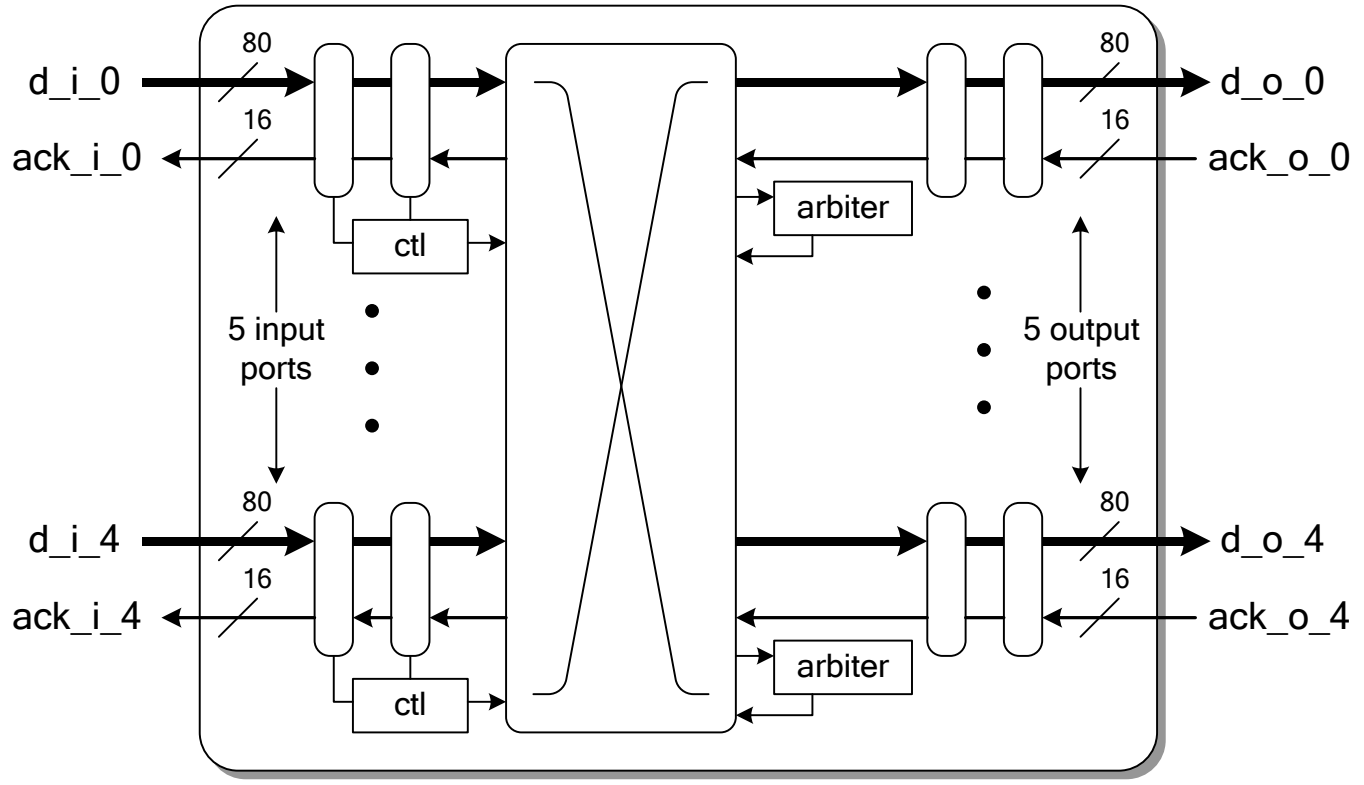
# ChSlice: implementation



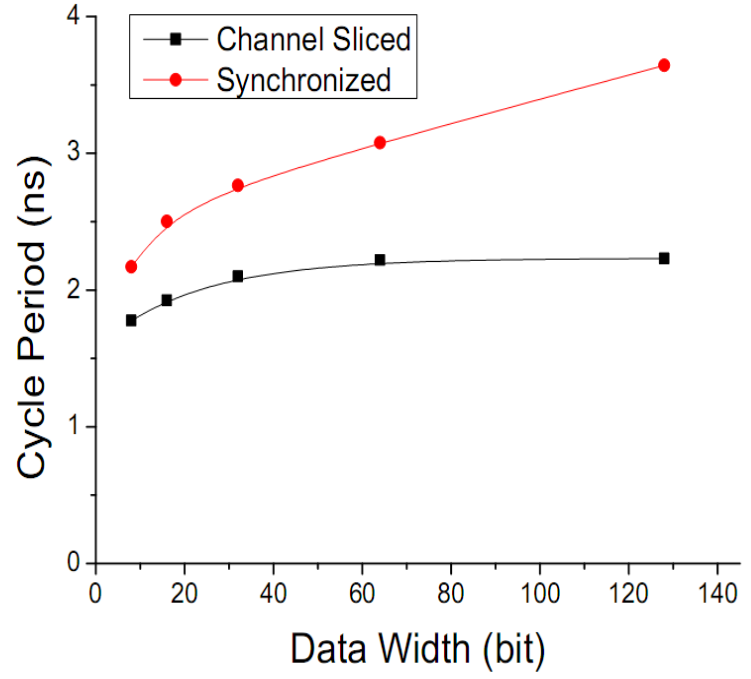
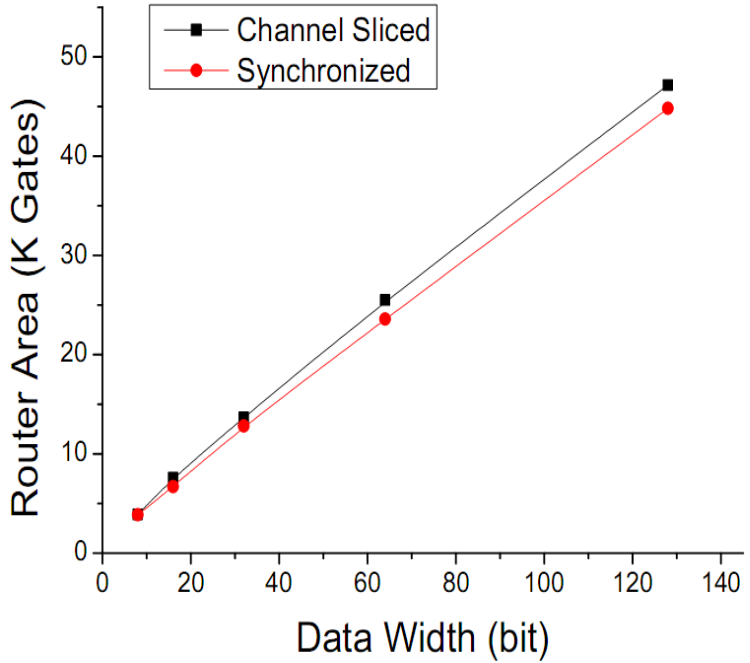
# Flow control



# Router: structure



# Speed and Area





# Future Work

- Implementation of a Spatial Division Multiplex (SDM) router (under test)
  - Switch structure
    - Clos Switch Networks
  - Path scheduling algorithm
    - random round-robin -> random arbitration
- Quality of Services support
  - Two switch structure in one router

# Publications

1. Wei Song and Doug Edwards. **Channel Slicing: a way to build fast routers for asynchronous NoCs.** *Proceedings of the UK Asynchronous Forum*, Sep. 2009.
2. Wei Song and Doug Edwards. **A low latency wormhole router for asynchronous on-chip networks.** ASP-DAC, 2010, in submission.
3. Wei Song and Doug Edwards. **Building asynchronous routers with independent sub-channels.** *Proc. of international Symposium on SOC*, Oct. 2009.
4. Wei Song, Doug Edwards, Jose Nunez-Yanez, and Sohini Dasgupta. **Adaptive stochastic routing in fault-tolerant on-chip networks.** NOCS, Pages 32-37, 2009.
5. Wei Song and Doug Edwards. **A dynamic link allocation router.** *Proceedings of the UK Asynchronous Forum*, Sep. 2008.

# Question?

# Compare with other routers

	Tech (nm)	Period (ns)	Period (Hz)	Pipeline Style	Other
Sliced Wormhole	130	2.2	450M	4-phase 1-of-4	Standard cell
Synchronized Wormhole	130	2.8	360M	4-phase 1-of-4	Standard cell
ANoC	130	4.0	250M	4-phase 1-of-4	Customized Cell Lib
ASPIN	90	0.88	1.13G	Dual-Rail / Bundled-Data	Customized Cell Lib
QNoC	180	4.8	208M	Bundled-data	Delay line
MANGO	120	1.26	790M	Bundled-data	Delay line
DSPIN	130	2.45	408M	Synchronous circuit	

# Crossbar, Benes, Clos

