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Channel Slicing: a Way to Build Fast Routers for Asynchronous NoCs

Wei Song and Doug Edwards

The University of Manchester

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Content

- Asynchronous NoCs
- Channel Slicing
  - Motivation
  - Sliced sub-channels
  - Flow control
- An asynchronous wormhole router
  - Implementation details
  - Performances

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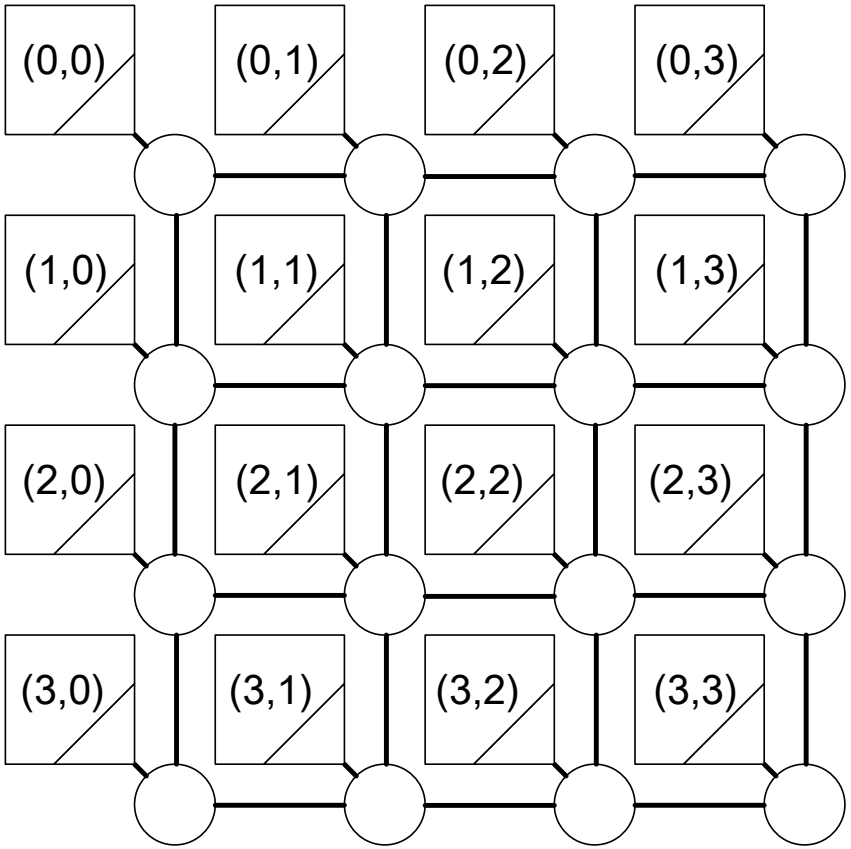
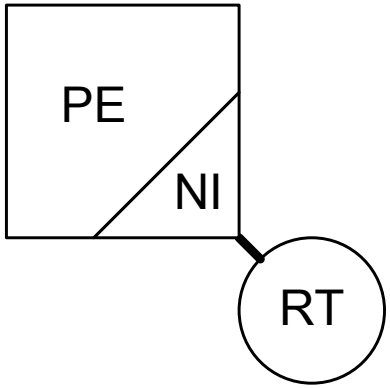
Network-on-Chip (NoC)





PE: Processor Element

NI: Network Interface

RT: router

Synchronous/Asynchronous

- Synchronous
  - Fast
    - Intel 80-tile 4GHz 65nm
    - DSPIN 408MHz 130nm
  - Small
    - DSPIN 0.161mm^2
  - Power Consuming
    - 10.39mW (250MHz)
  - Sensitive to variation
  - Complex clock tree
- Asynchronous
  - Slow !!
    - ASPIN 714MHz 90nm
    - ANoC 220MHz 130nm
  - Large
    - ANoC 0.211mm^2
  - Power Efficient
    - 3.69mW (160MHz)
  - Tolerance to variation
  - No clock tree

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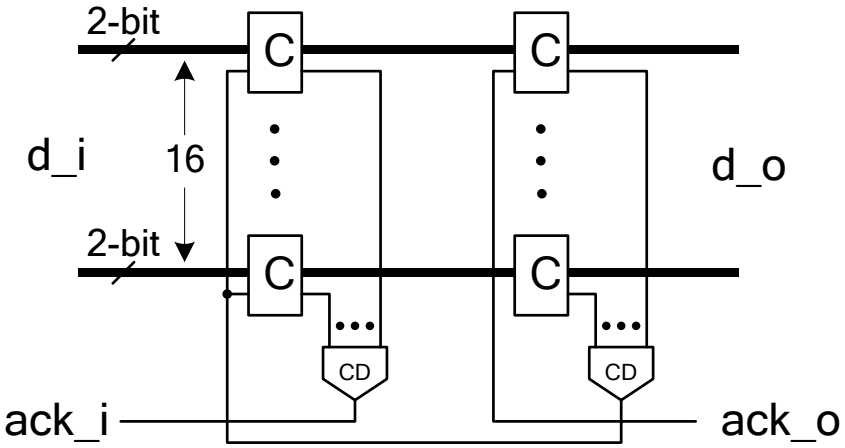
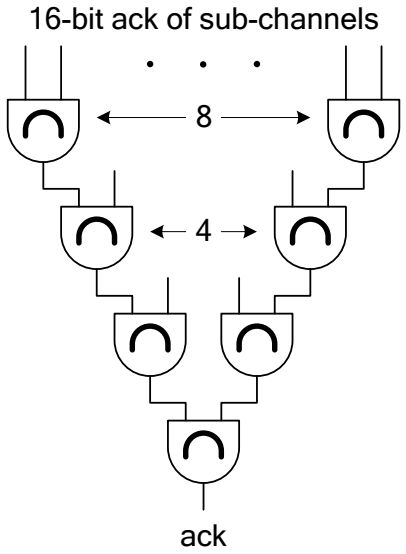
Asynchronous Pipelines

- CHAIN (*Bainbridge'02*)
  - 4 phase 1-of-4 pipelines
- QoS NoC (*Felicijan'04*)
  - 8-bit, Four 4 phase 1-of-4 pipelines
- ANoC (*Beigne'05*)
  - 32-bit 16 4 phase 1-of-4 pipelines
- SpiNNaker (*Plana'07*)
  - Several 1-of-4/2-of-7 pipelines
- ASPIN (*Sheibanyrad'08*)
  - 32-bit 16 dual-rail pipelines / bundled-data
- MANGO (*Bjerregaard'05*) & QNoC (*Dobkin'09*)
  - Bundled-data

Completion Detection

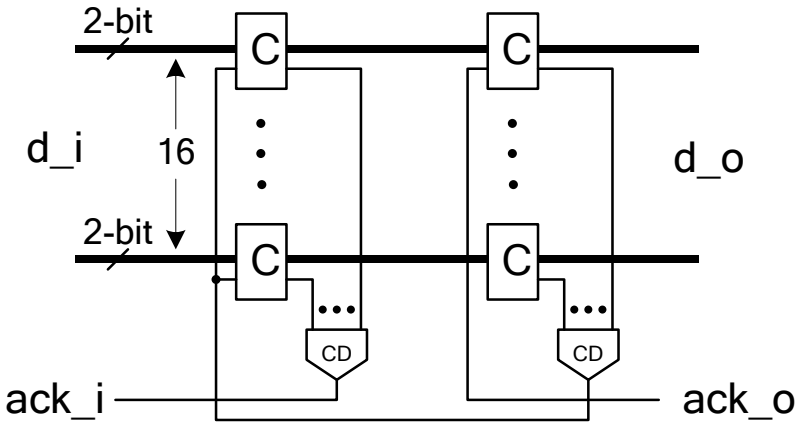


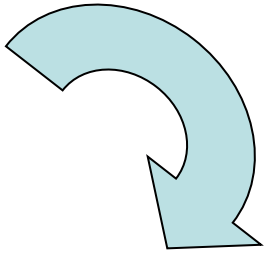


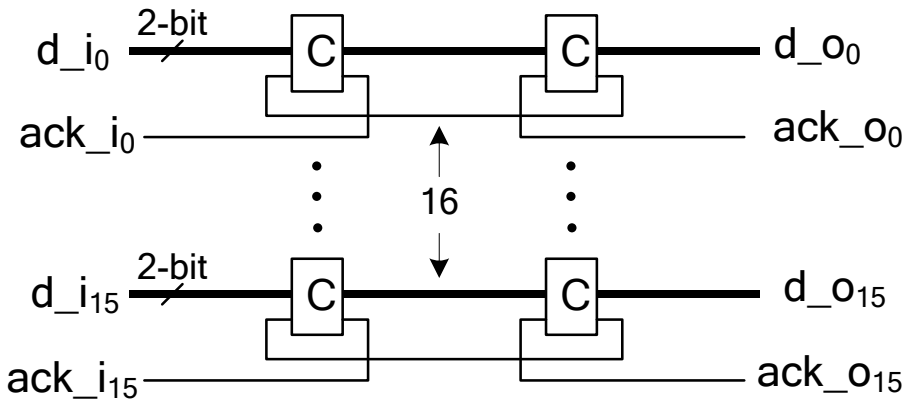
Advantages: data on all sub-channels are synchronized, ease the time division multiple access (TDMA) techniques, such as virtual channel and TDMA

Drawbacks: low speed (66% on CD)

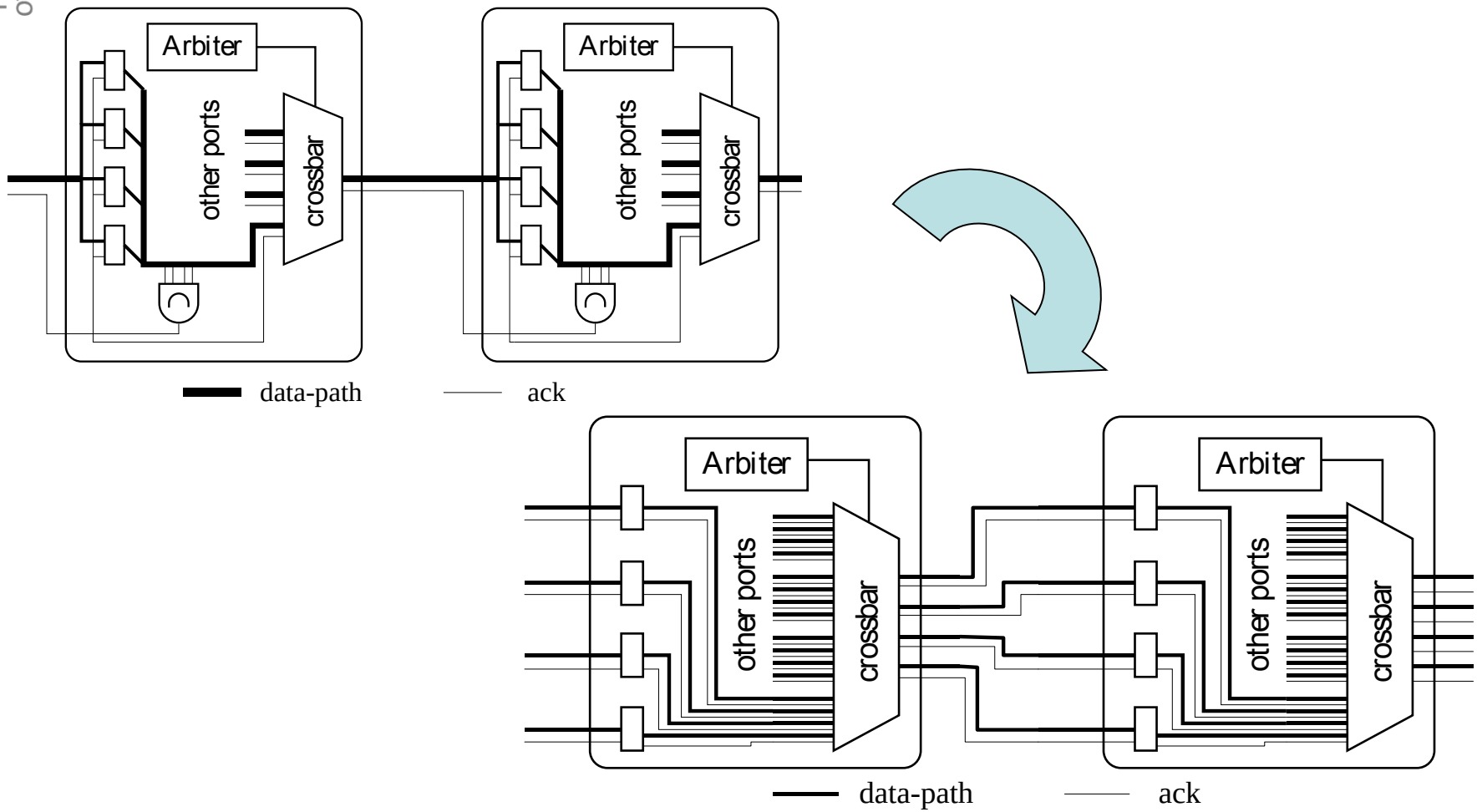
ChSlice: implementation



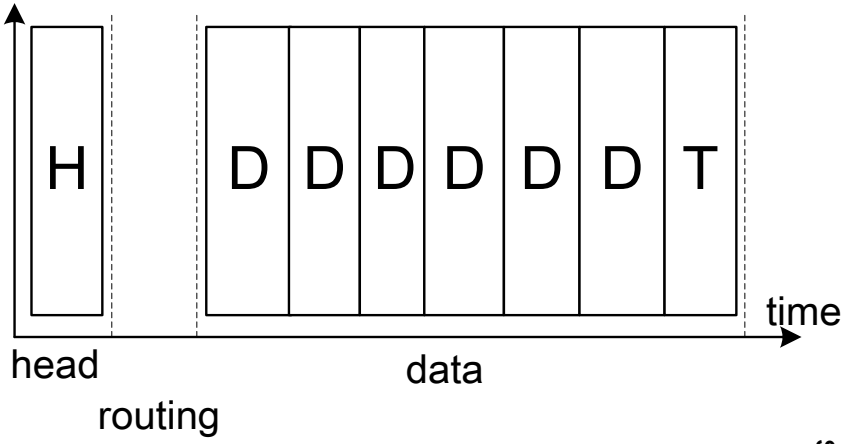


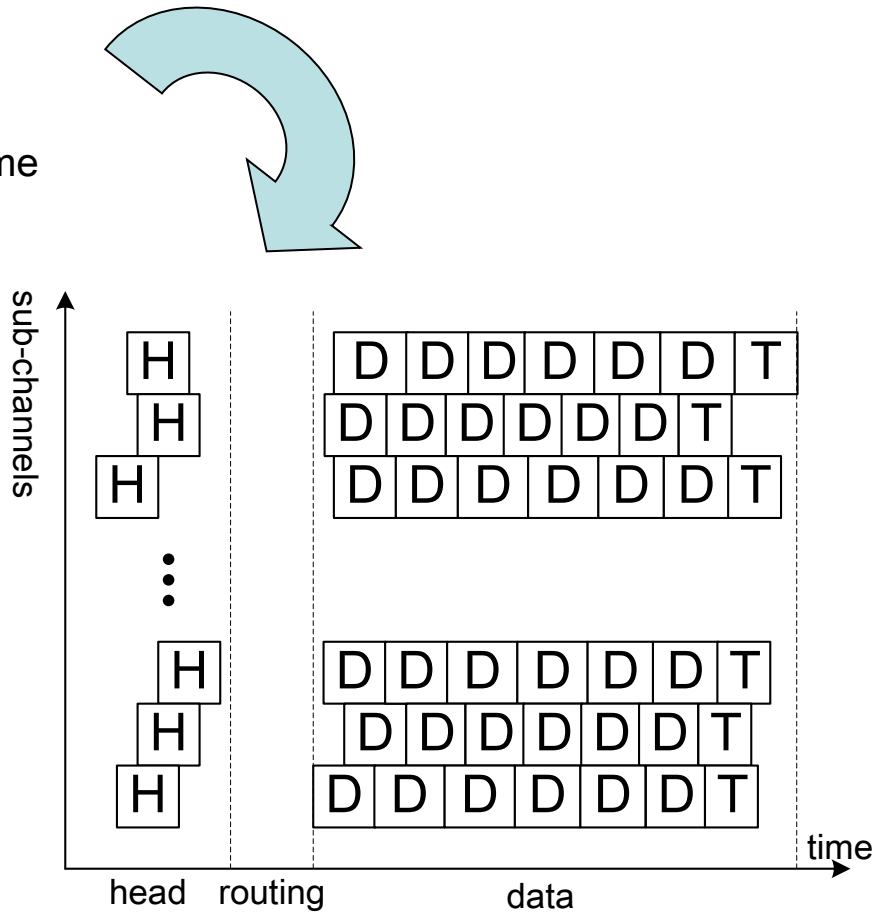


How to do it in a router?



Flow control





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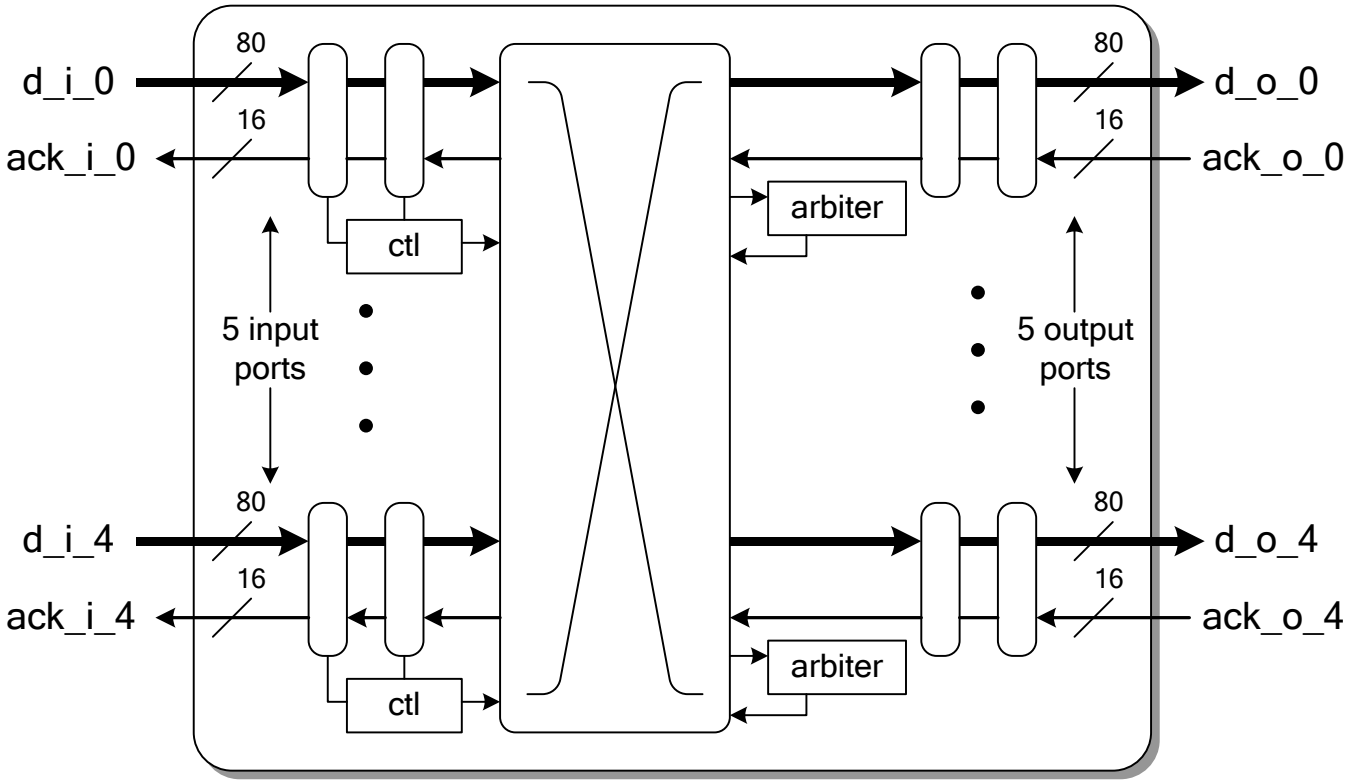
Router: structure



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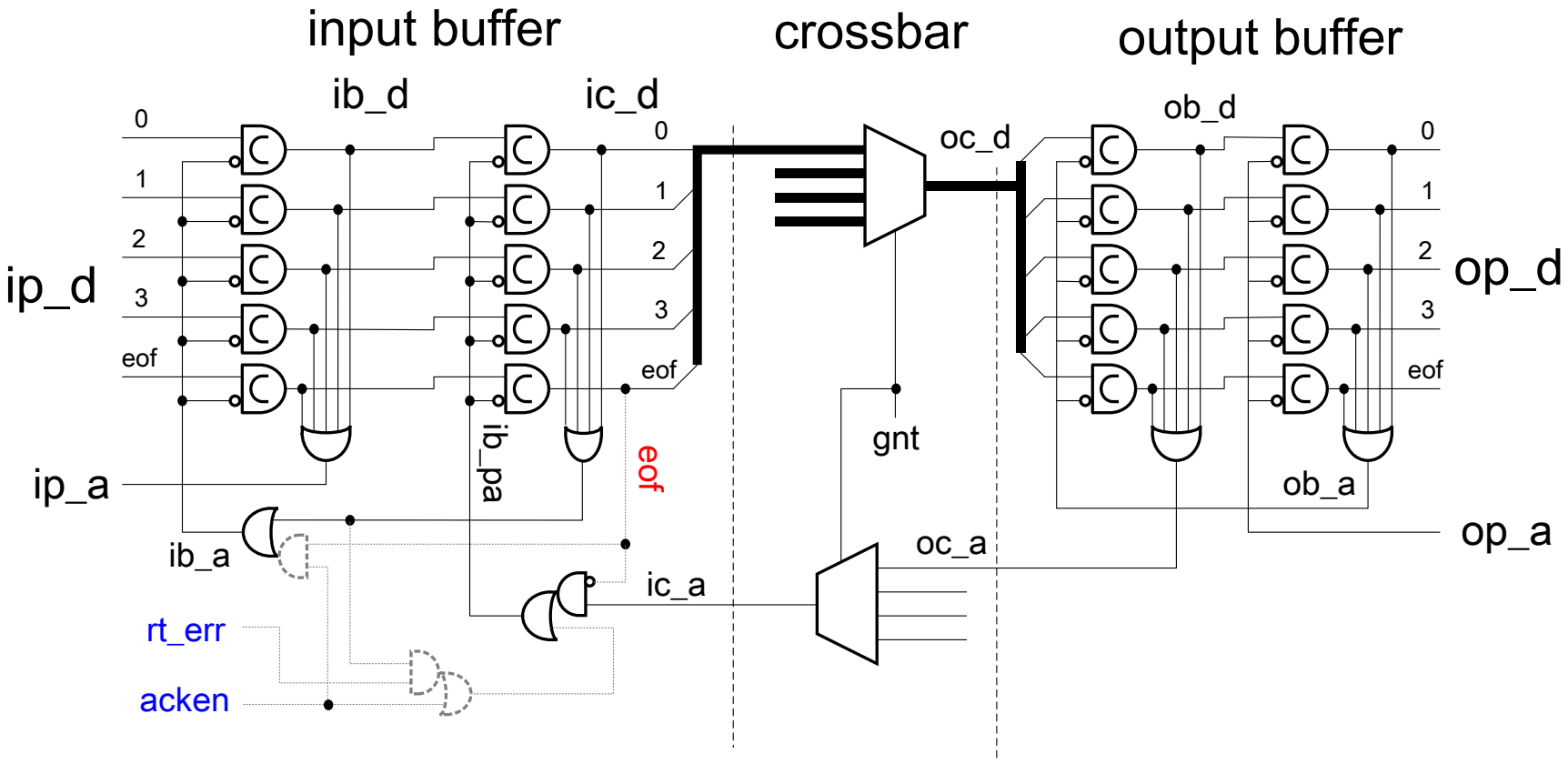
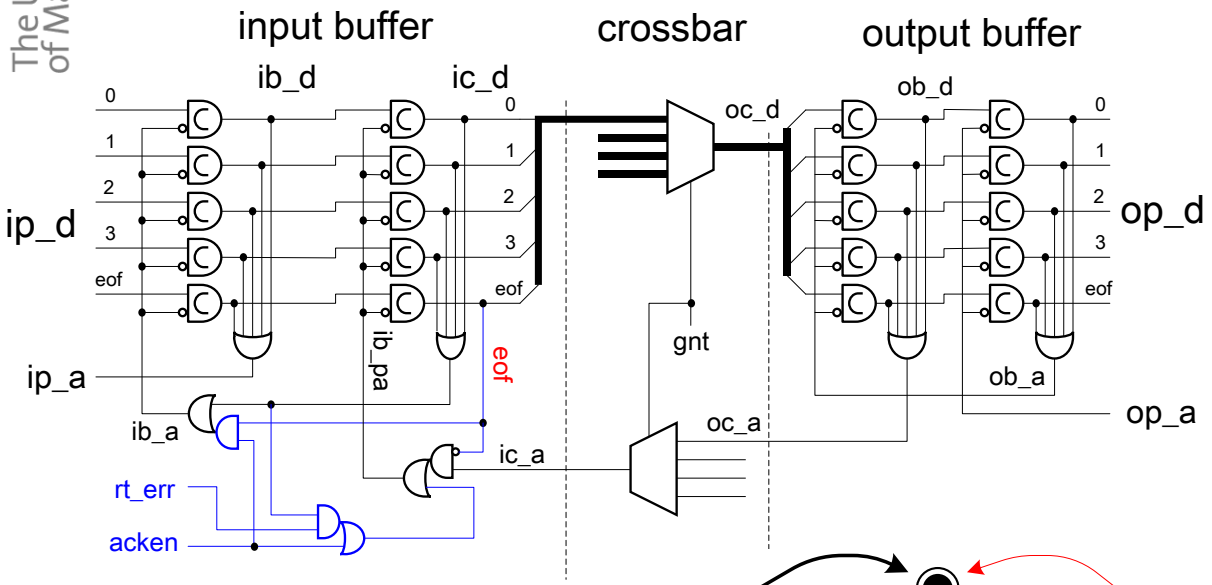
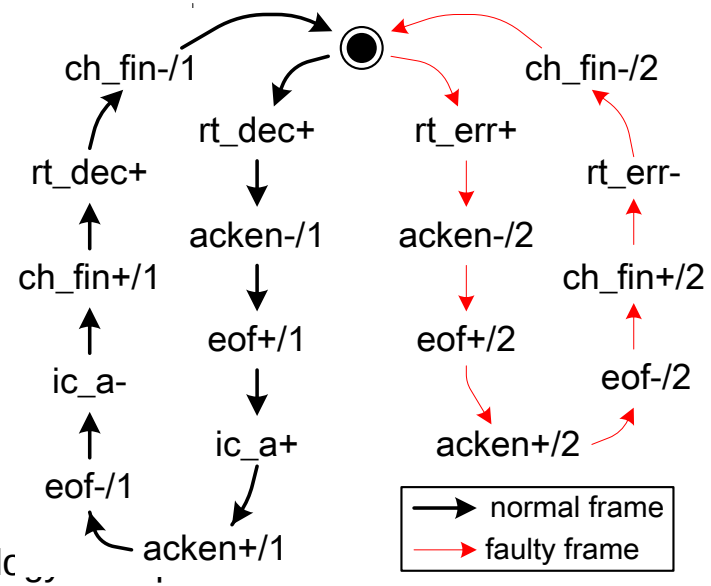
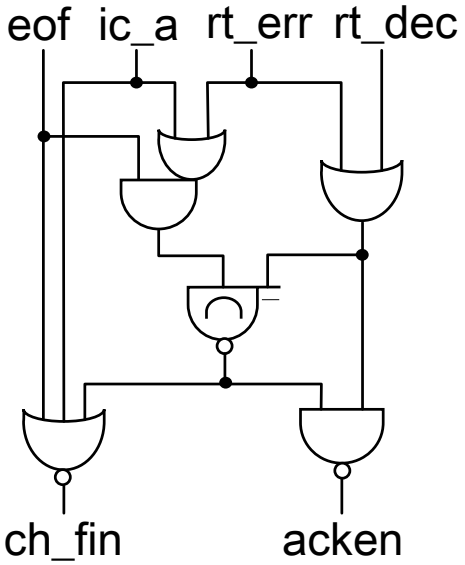
Router: data path



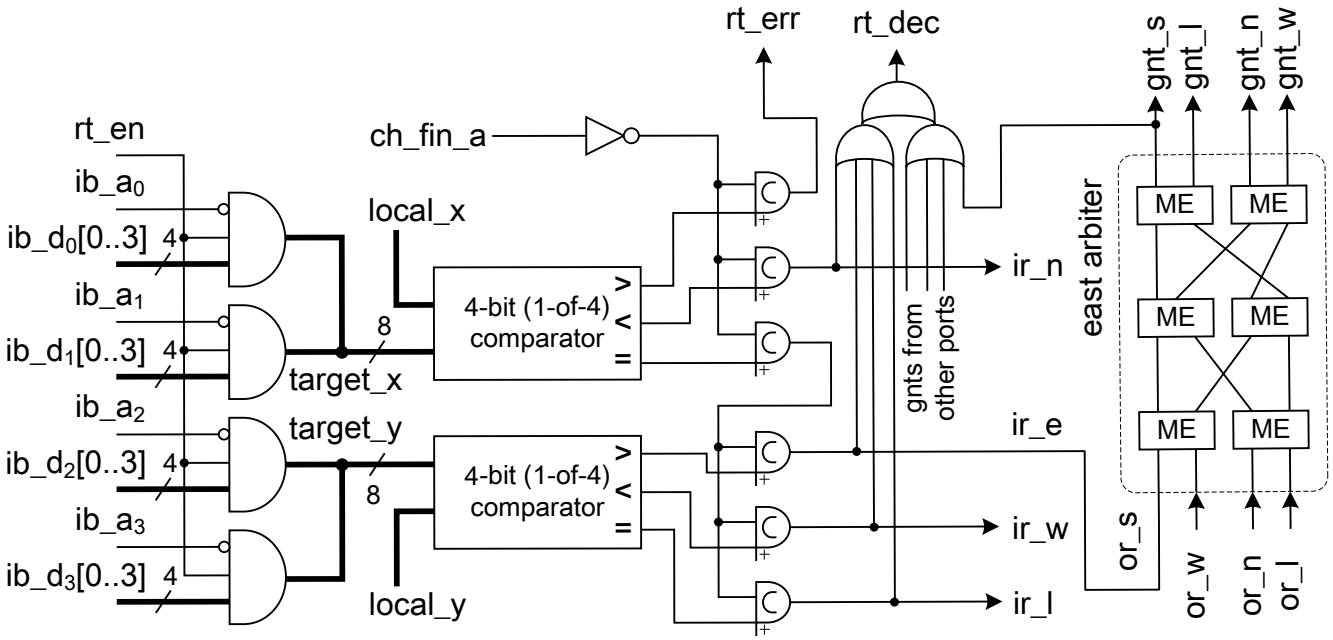
Re-Synchronization

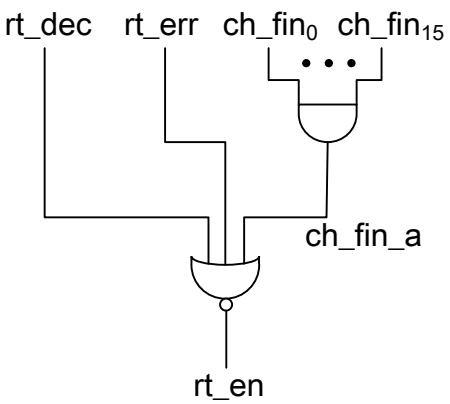


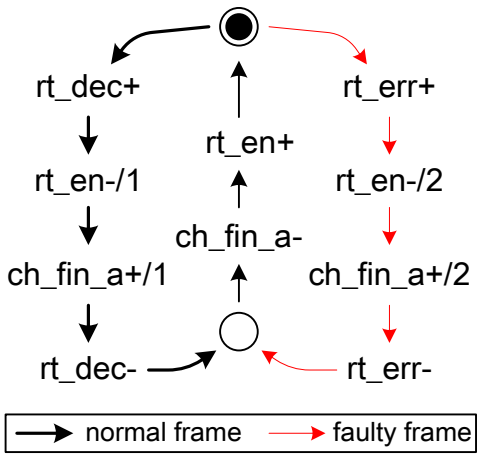




Routing Decision







Router: layout

- Faraday 130nm Technology
- 32-bit, 5 ports, XY routing algorithm
- 0.3x0.3mm (12.6K gates, 0.050mm^2)
- Typical corner (25 ^{o}C 1.2V)
- Cycle period 2.2 ns (1.82GByte/s per port)
- Equivalent to 450MHz

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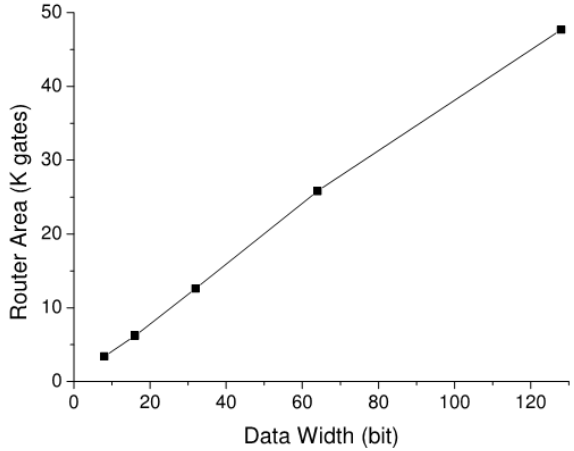
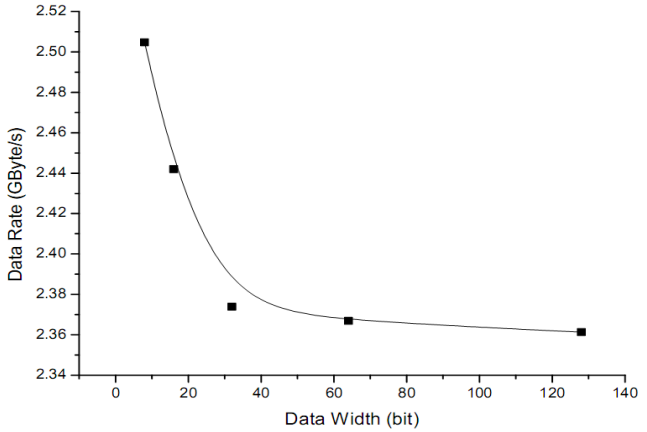
Compare with other routers

	Tech (nm)	Period (ns)	Period (Hz)	Pipeline Style	Other
Sliced Wormhole	130	2.2	450M	4-phase 1-of-4	Standard cell
Synchronized Wormhole	130	2.8	360M	4-phase 1-of-4	Standard cell
ANoC	130	4.0	250M	4-phase 1-of-4	Customized Cell Lib
ASPIN	90	0.88	1.13G	Dual-Rail / Bundled-Data	Customized FIFO
QNoC	180	4.8	208M	Bundled-data	Delay line
MANGO	120	1.26	790M	Bundled-data	Delay line
DSPIN	130	2.45	408M	Synchronous circuit	

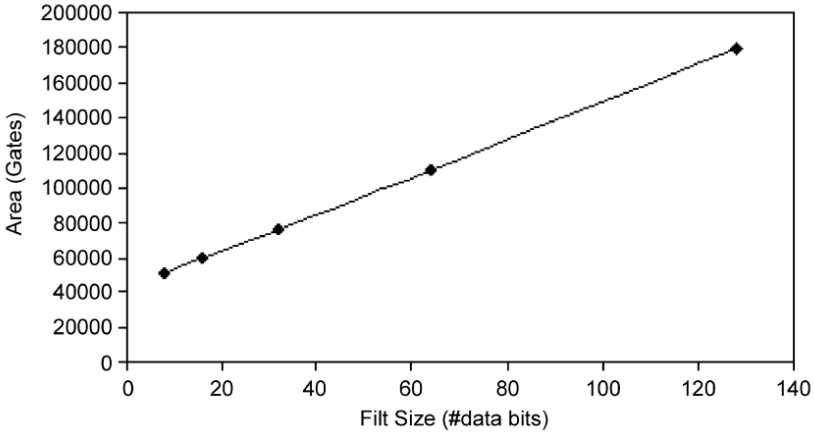
Speed vs. Data Width

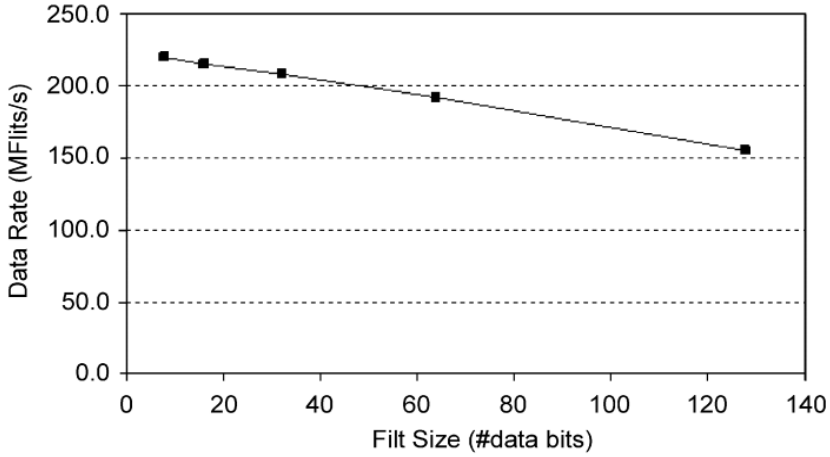
Sliced Wormhole



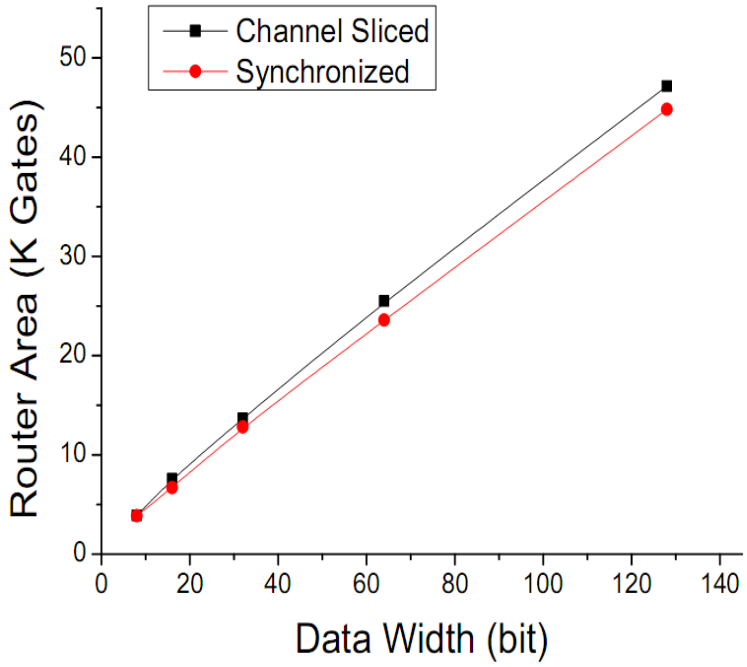


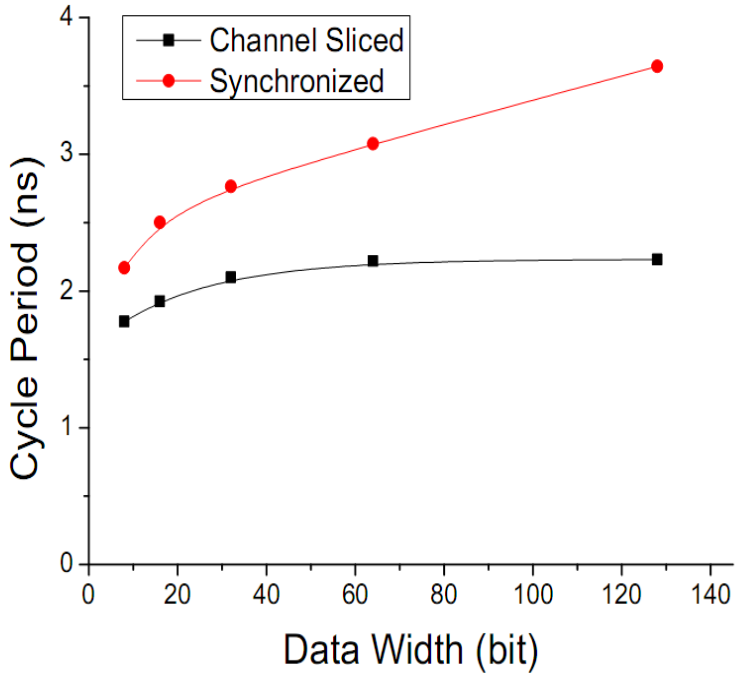
QNoC





Speed and Area





Question?