Untethering the RISC-V Rocket Chip

-- A code release from the lowRISC project

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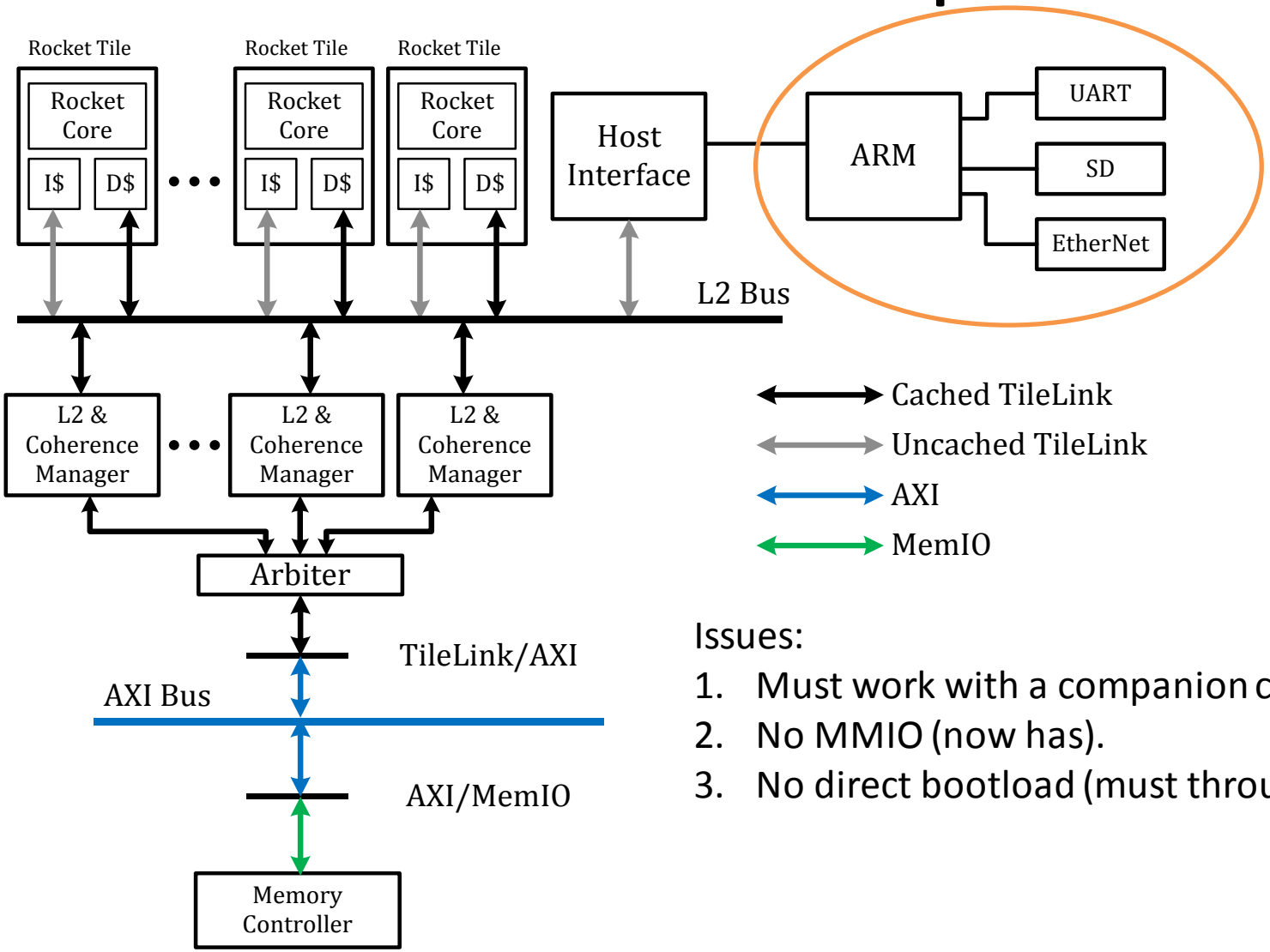
Background

- Rocket-chip
  - An open-source SoC from UC Berkeley
  - Rocket core
    - RISC-V 64 ISA
    - 5/6 stage single-issue in-order processor
- lowRISC
  - An opensource SoC provider

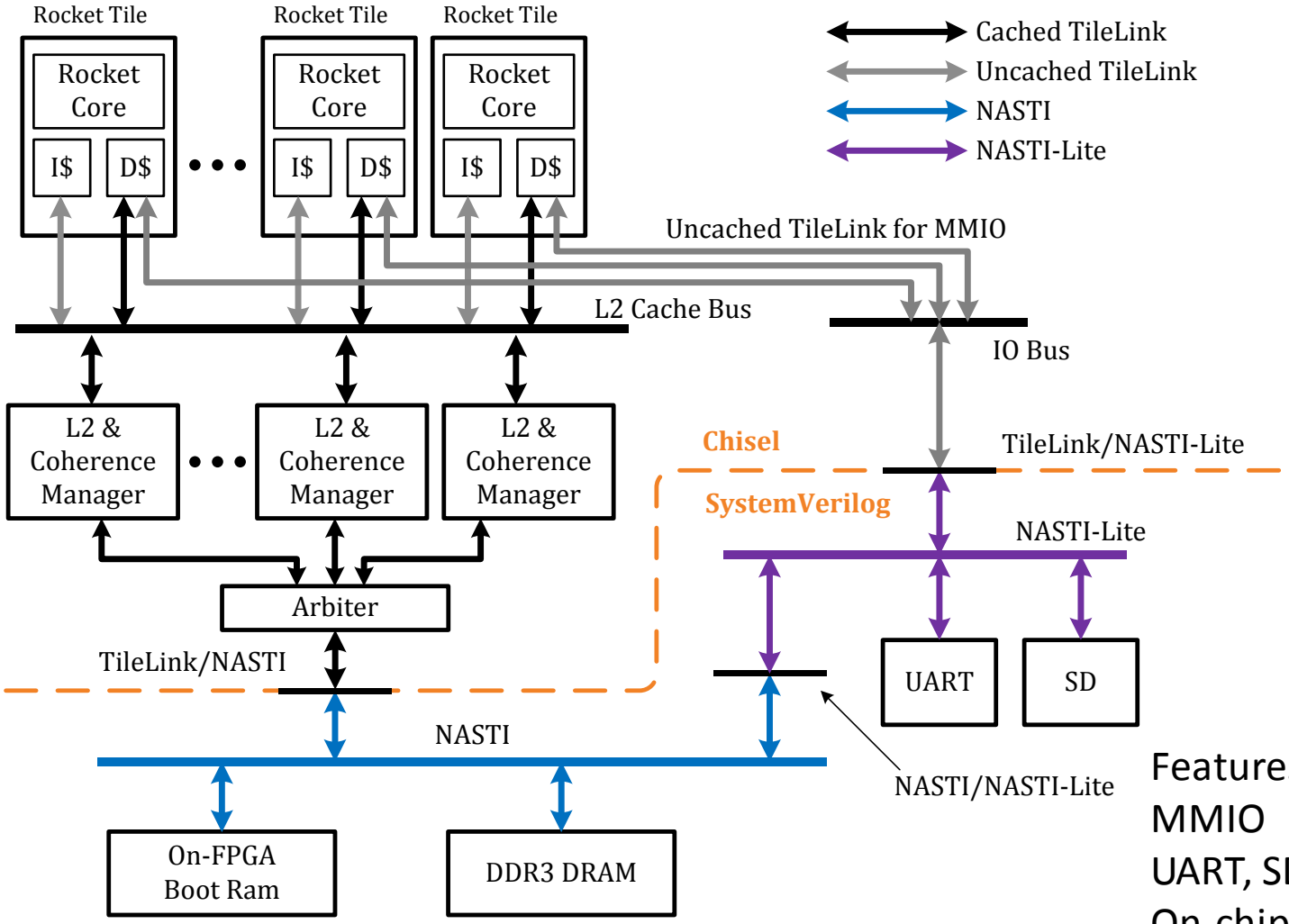
Rocket Chip



Issues:

1. Must work with a companion core (ARM).
2. No MMIO (now has).
3. No direct bootload (must through ARM).

Untethered Rocket Chip



Features:
MMIO
UART, SD, DDR3, Boot RAM
On-chip NASTI interconnect in SystemVerilog

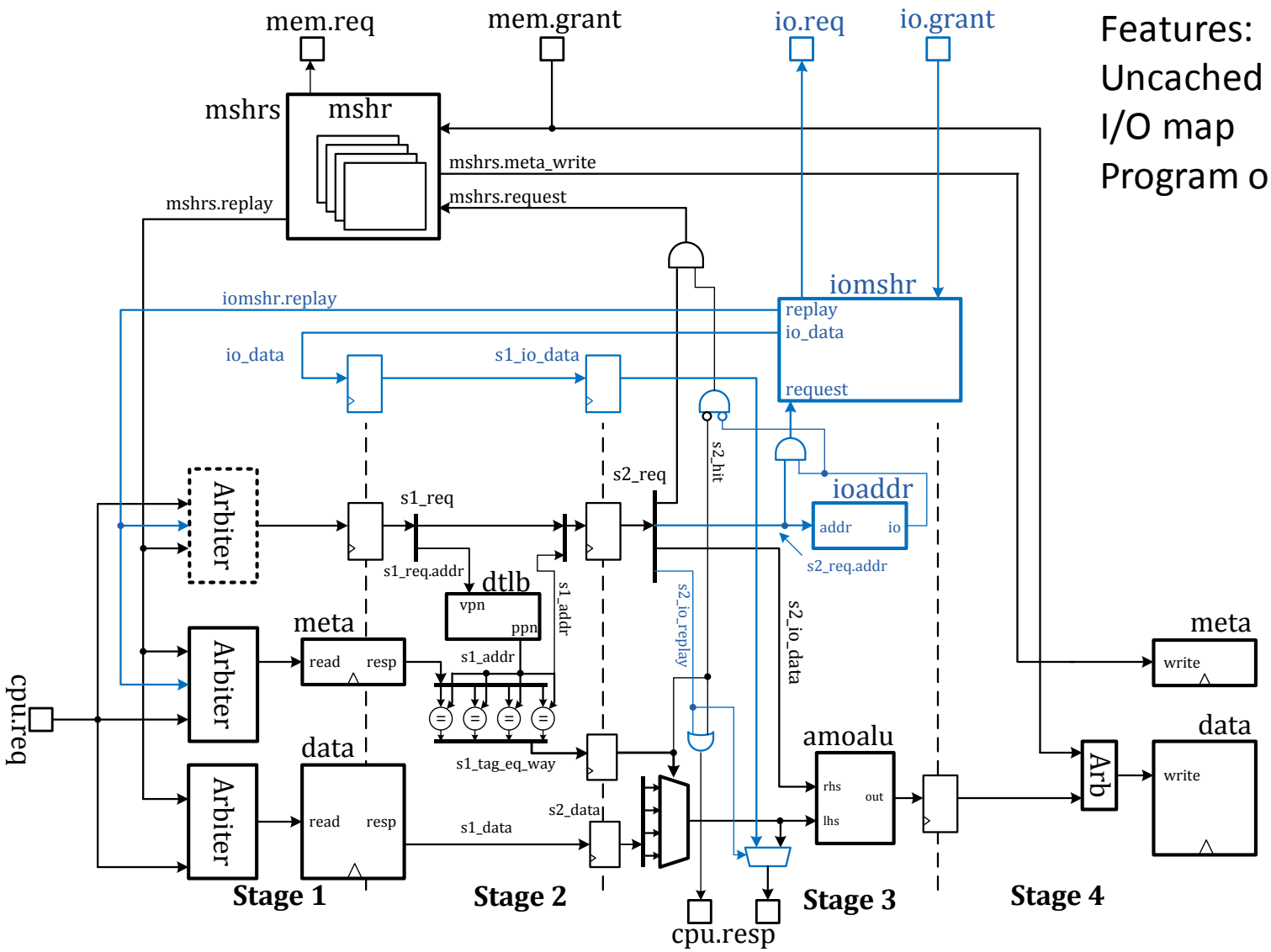
I/O and Memory Map

- I/O map
  - 4 I/O sections
  - CSR: io_base, io_mask, io_update

    hit = (addr & ~io_mask) == io_base
- Memory map
  - 4 memory sections
  - CSR: mem_base, mem_mask, mem_phy, mem_update

    hit = (addr & ~mem_mask) == mem_base
    addr' = (addr & mem_mask) | mem_phy

MMIO



Features:
Uncached (bypass L1 & L2)
I/O map
Program order

Bootloader

- Two stage bootloaders
  - First stage bootloader
    - Copy the second stage bootloader to DDR RAM
    - Uncached copy (mapping DDR RAM to IO)
    - Re-map DDR RAM to memory address 0
    - Reset Rocket
  - Second stage bootloader
    - Revised Berkeley bootloader (BBL)
    - Driving I/O devices
    - Start multi-core, VM support
    - Load and boot RISC-V Linux in virtual address space

A Code Release

- The untethered Rocket chip has been released.
  - A tutorial: http://www.lowrisc.org/docs/untether-v0.2/
  - Code repo https://github.com/lowRISC/lowrisc-chip
- Key Features
  - FPGA demo with RISC-V Linux
    - Xilinx Kintex-7 KC705 suite (developing system)
    - Digilent NEXYS4-DDR board (low-end board) 320 USD
  - Up-to-date Rocket code from Berkeley
    - Merged all updates up to October 2015.
  - Nearly free development environment
    - Replace VCS with **Verilator**/ISim
    - Voucher or **WebPACK** Vivado license

Summary of the Code Release

- Remove host target interface
- Add reconfigurable I/O and memory maps
- Add memory mapped IO
- Rewrite TileLink/NASTI interfaces
- Provide on-chip NASTI interconnects
- Integrate DDR2/3 controller, SD (FAT32), UART
- 2 bootloader
- New design environment using free tools
- New make files and scripts

- Tagged memory to be re-integrated
- No support for Zedboard

http://www.lowrisc.org/docs/untether-v0.2/release/

Future Works

- Looking for help to remove HTIF in RISC-V Linux
- Re-integrate tagged memory
- Add an interrupt controller
- Add trace debugging (with help from Stefan Wallentowitz)
- Add run-control debugger (SiFive)
- Platform spec

- For more information

  Visit http://www.lowrisc.org/