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NoRC Project Meeting Report

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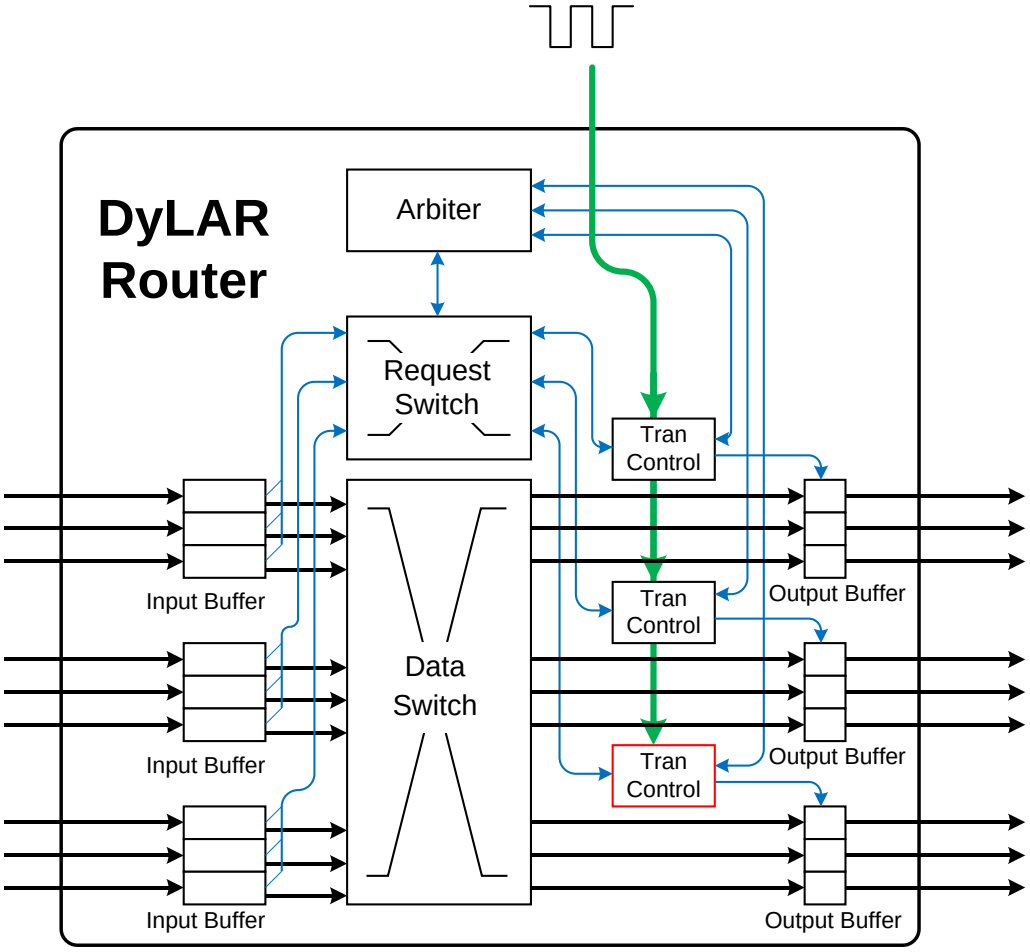
23-Mar-2009

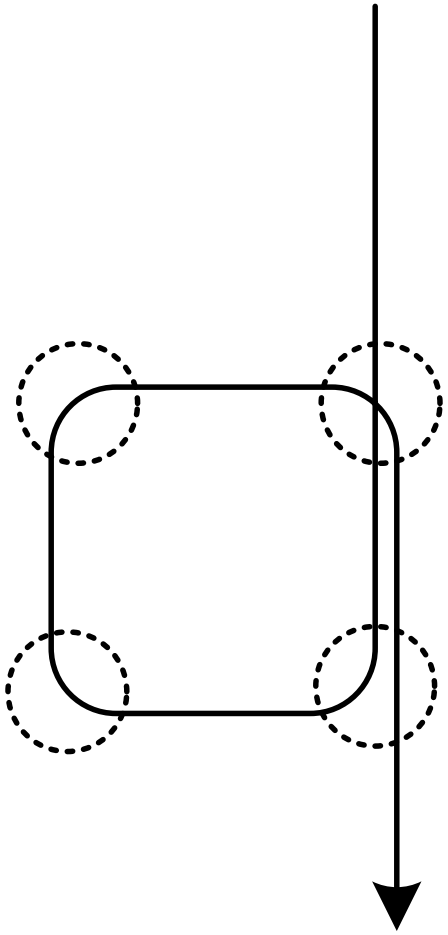
Content

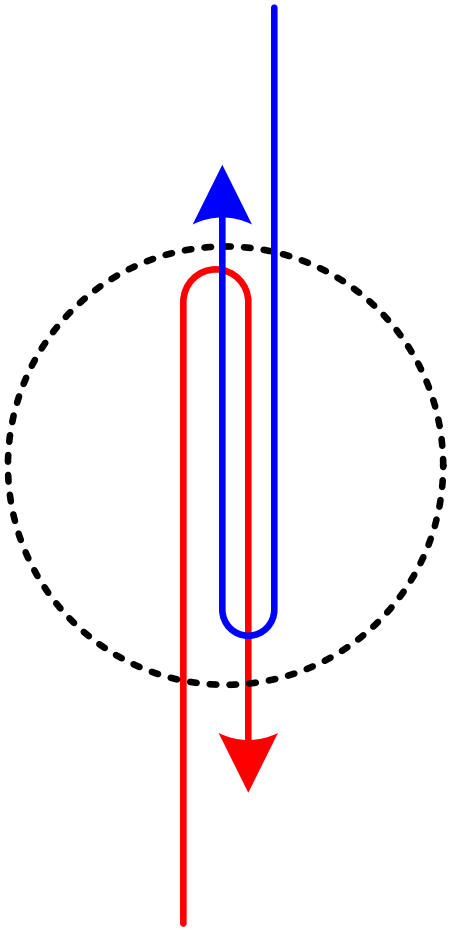
- Avoid deadlocks in the Dynamic Link Allocation Routers
- Delay measurements of asynchronous channels

The original design



The possible deadlocks

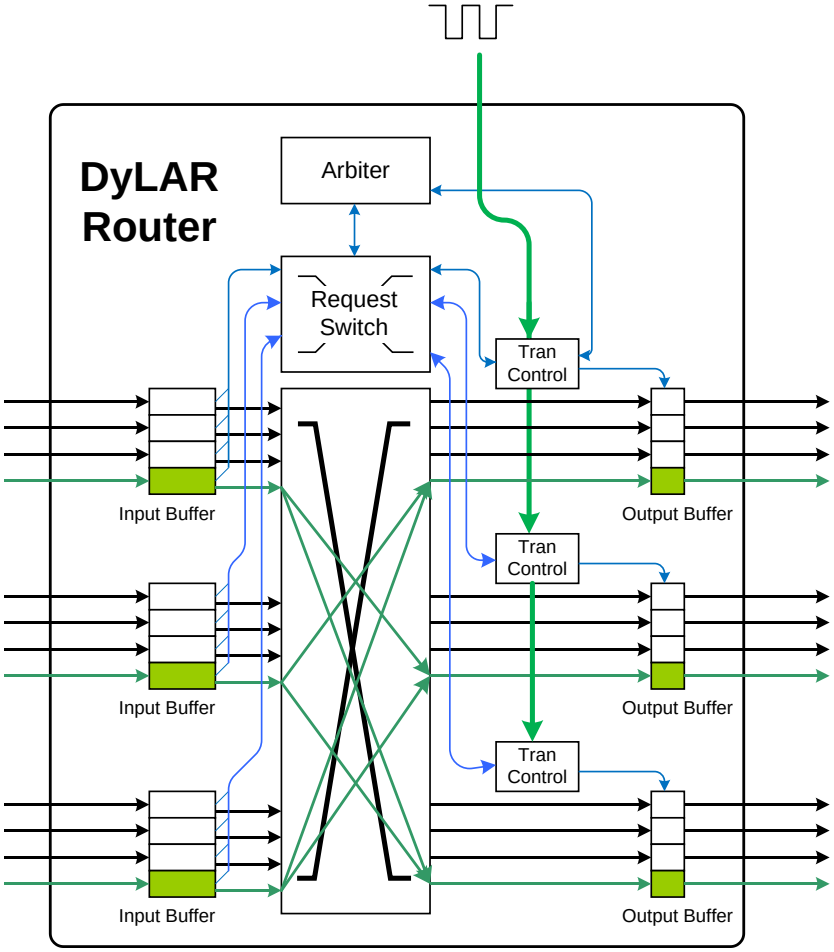




Deadlock avoidance in fault-free NoCs

- Restrict loops
  - Constrain the number of request lines that sharing the physical channels
- Divide the forward/backward (request/ack) channels

The new router



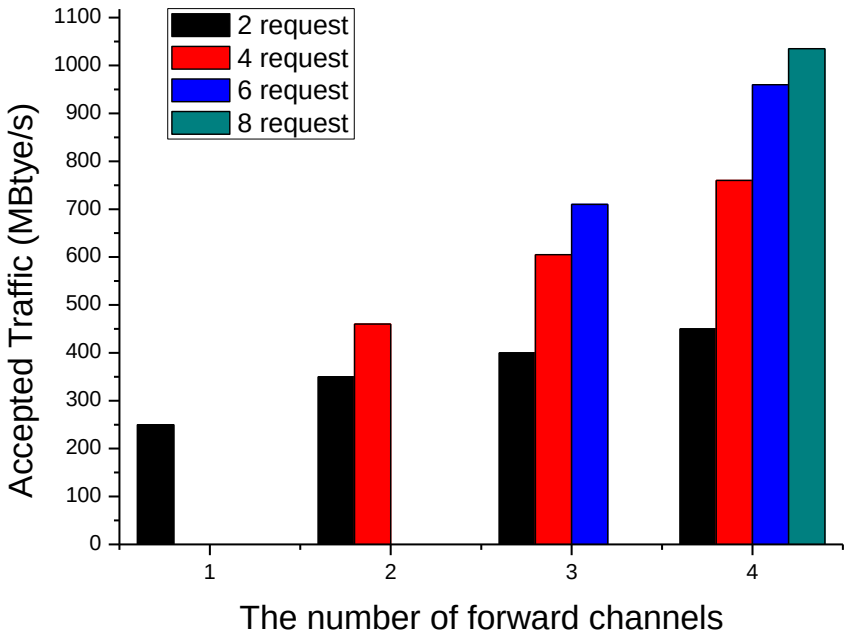
Proof of deadlock-free

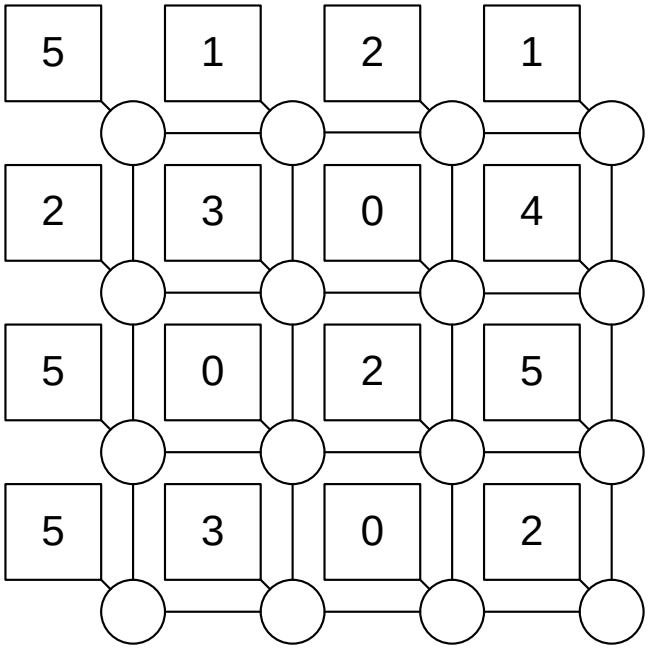
- Forward paths is a SDM network
  - Routing algorithm has loops
  - The maximal loop is restricted by request number which equal with channel number
- Backward paths is a wormhole network
  - Routing algorithm has loops
  - Frame length is 1
  - The maximal number of frames in a single router is the request number
  - Deadlock-free when the input buffer is large enough

Benefits of this modification

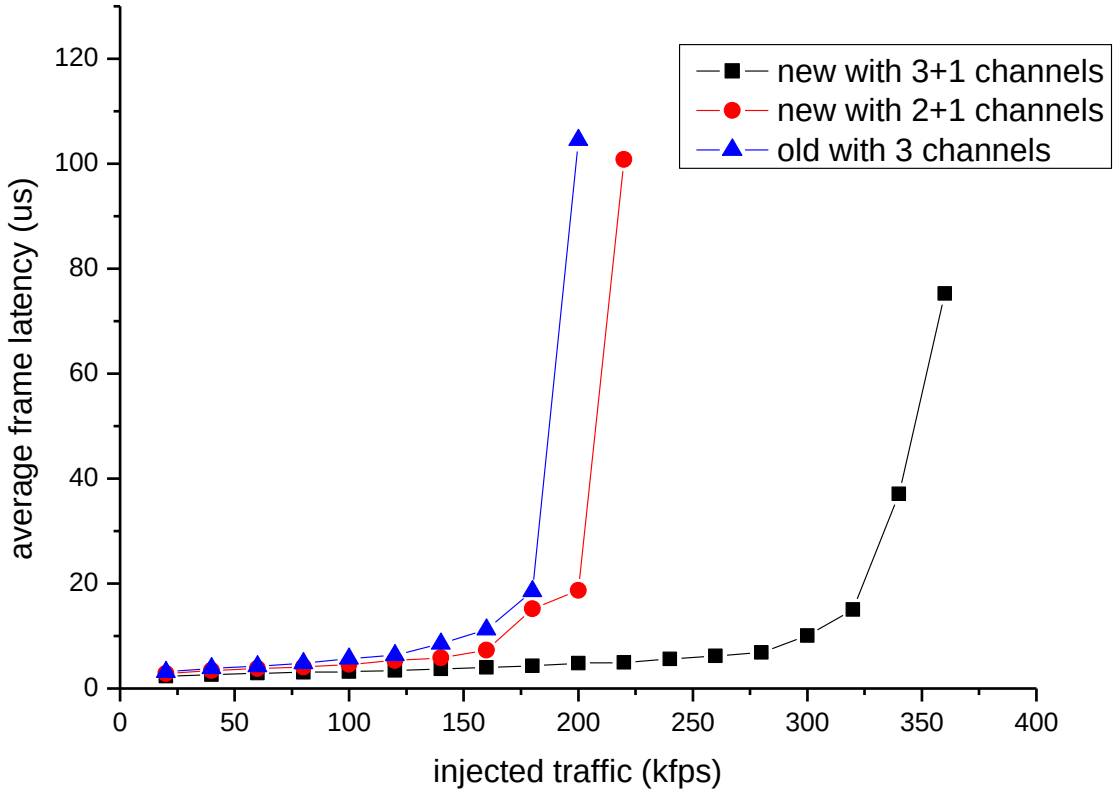
- Deadlock free in any fault-free NoCs.
- Support a maximal number of (N-1)*2 requests on a physical channel.
- Reduce the complexity of router and network interface designs.

Some simple results





Some simple results



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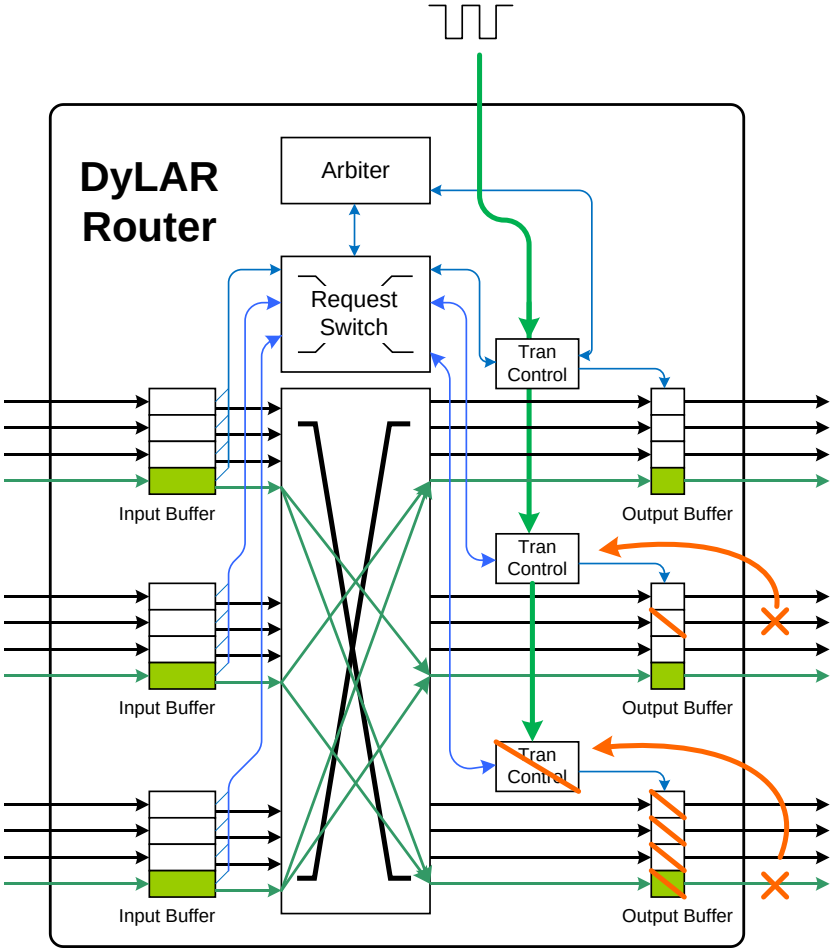
On faulty NoCs



- Avoid deadlocks in the Dynamic Link Allocation Routers
- Delay measurements of asynchronous channels

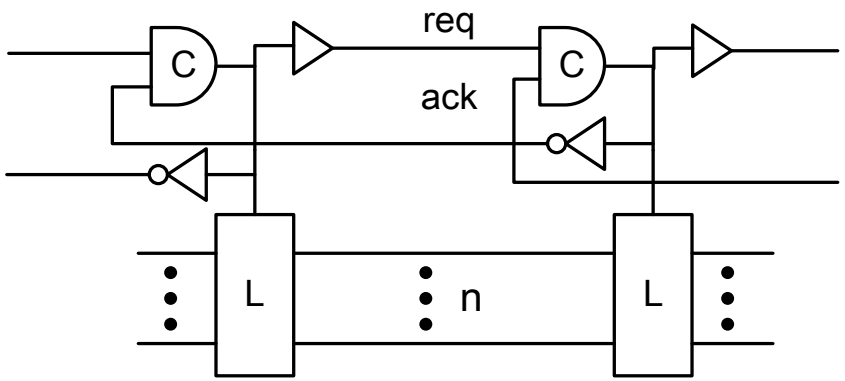
Purpose

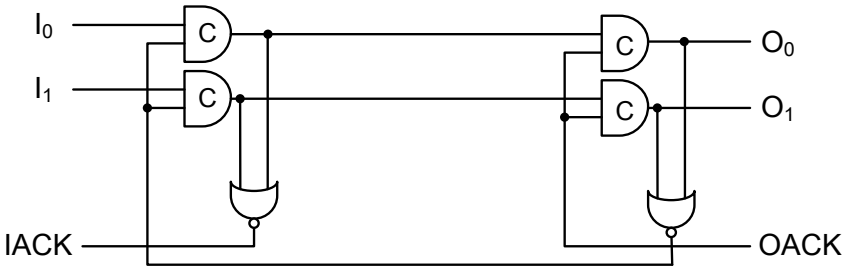
- Measure the latency of different asynchronous channels under <50 nm technology
- Try to prove that serial channels are faster than parallel channels and measure how fast they are

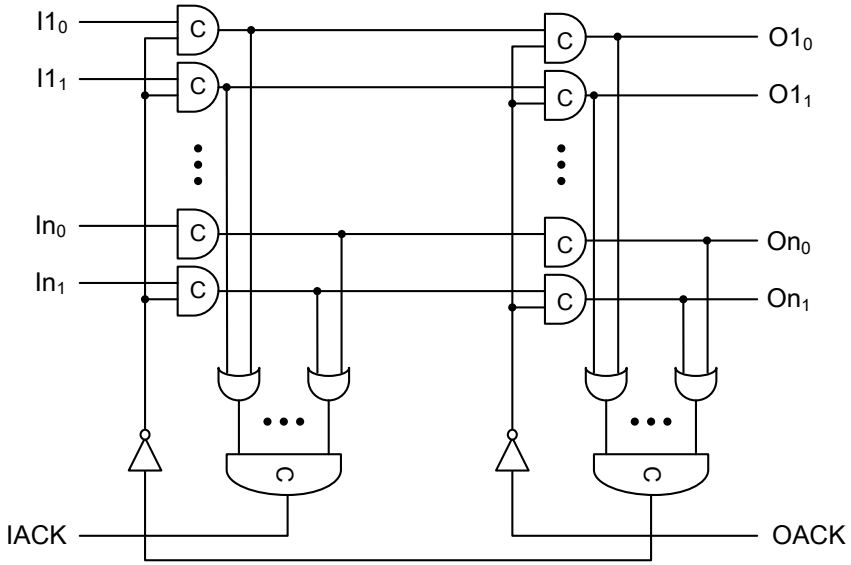
Other ANoC Designs

- Current ANoC designs are using parallel channels
  - MANGO bundled data
  - QNoC bundled data
    synchronized 4-phase channels
  - ANoC synchronized 4-phase channels

Asynchronous Channels







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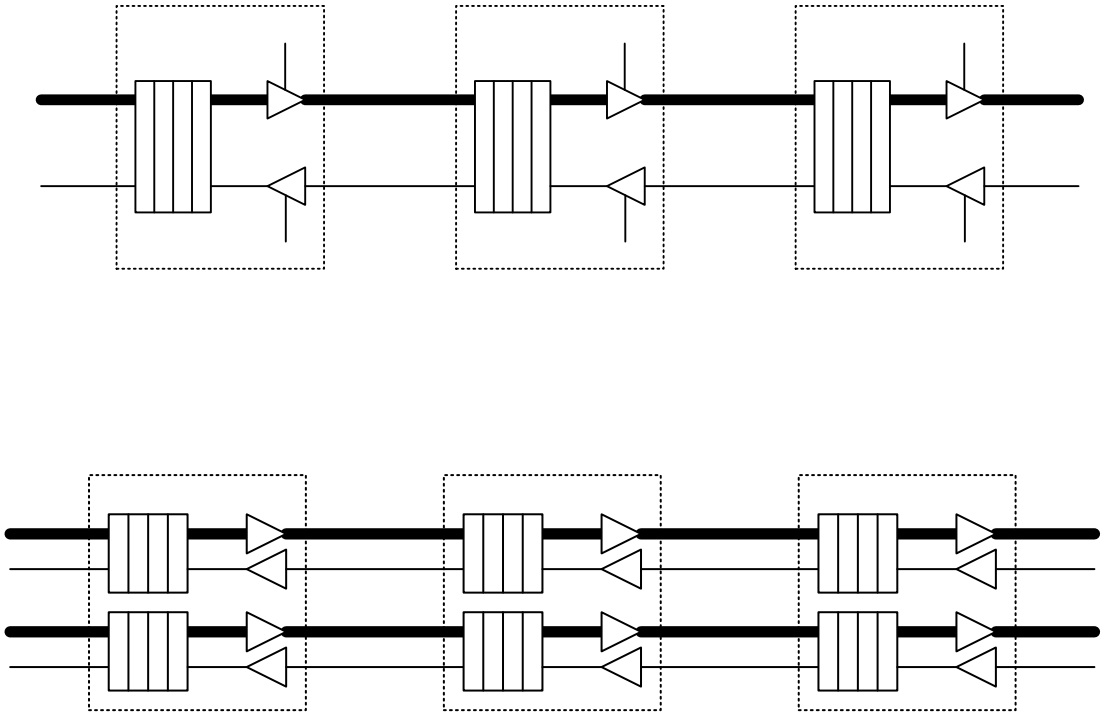
Channels in NoCs



Measurement procedure

- Cell Library
  - Nangate 45nm Open Source Cell Library
  - 32 bit, 4 8-bit serial channels
- Tool Flow
  - Verilog netlist
  - DC
  - SoC encounter
  - Calibre LVS/xRC -> HSpice netlist
  - NanoSim

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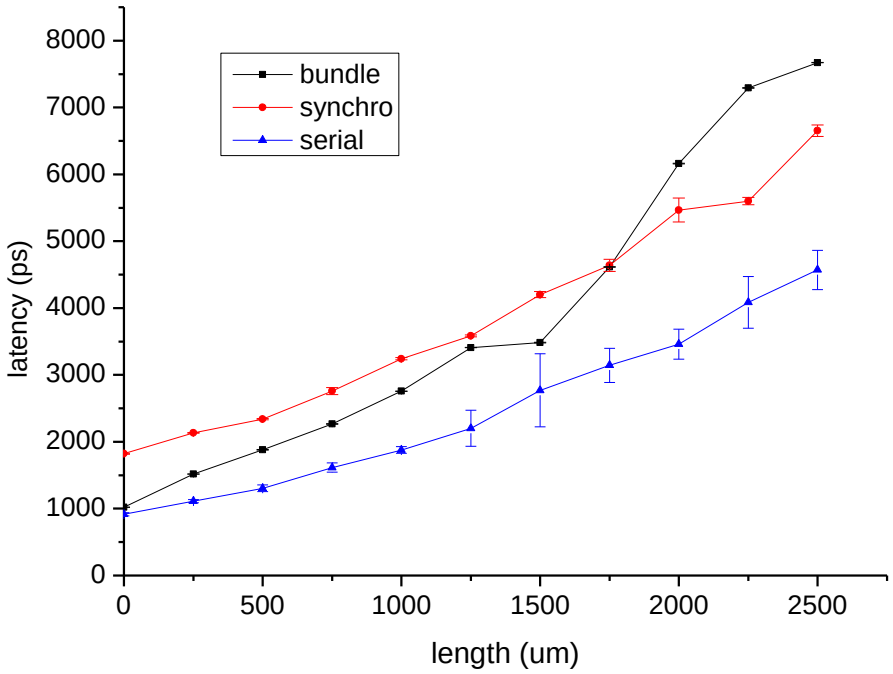
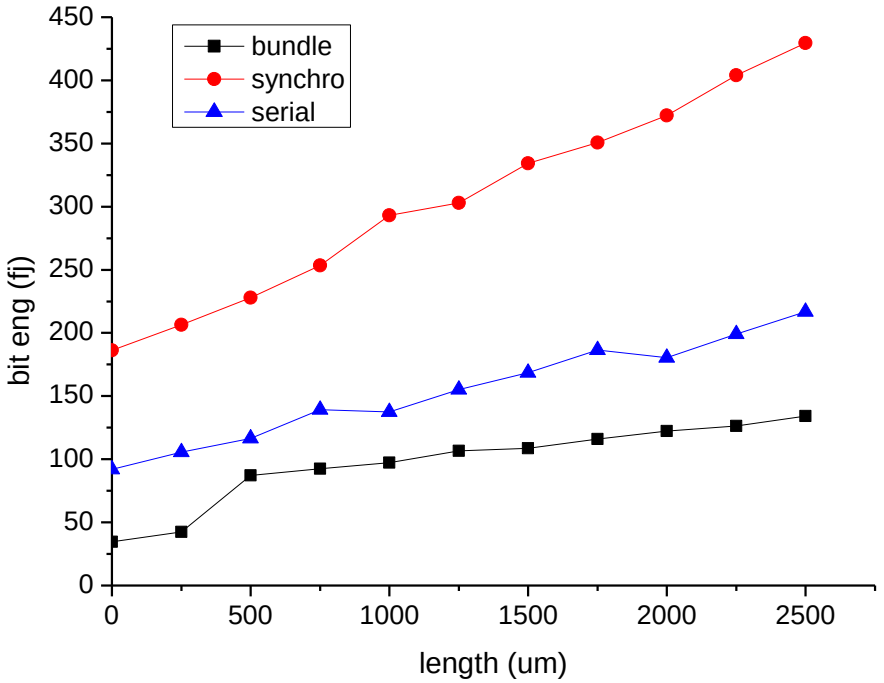
Loop Delay and Bit Energy

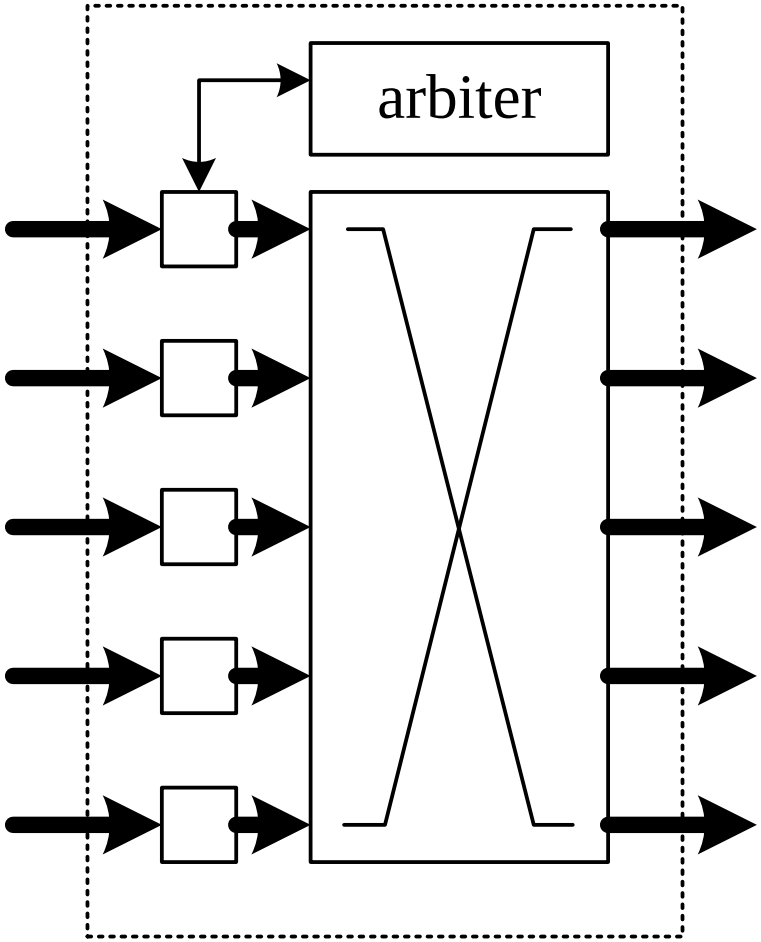




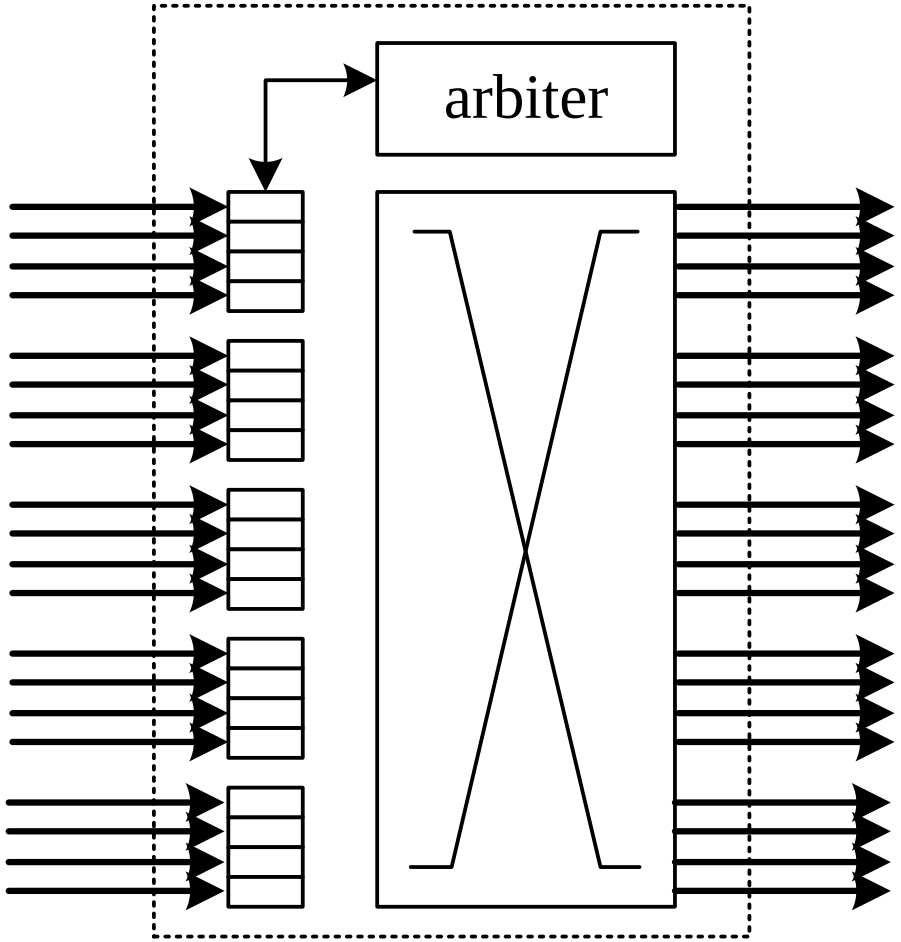
Comparing in NoCs

- Compare traditional wormhole routers with routers with 4 sub-channels
- Set the channels length to 1mm according to the 45nm technology
- XY routing algorithm is used
- Target address is encode into 8 bits

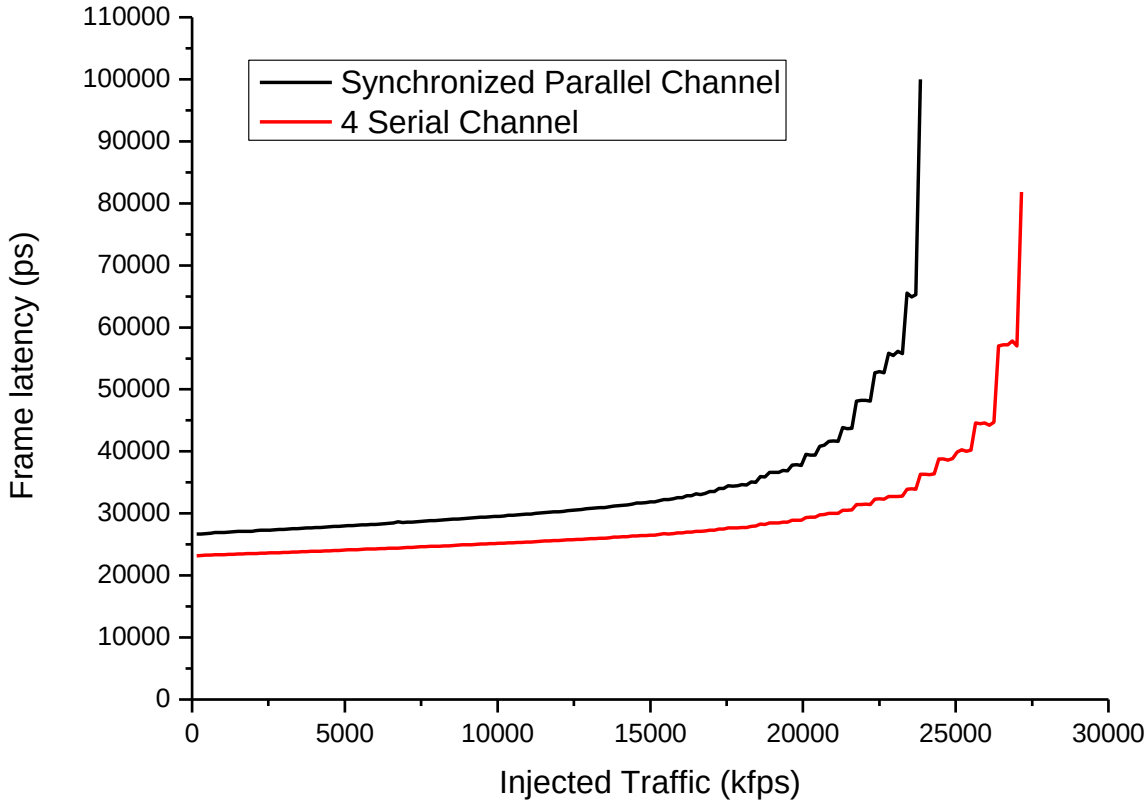
The traditional wormhole router



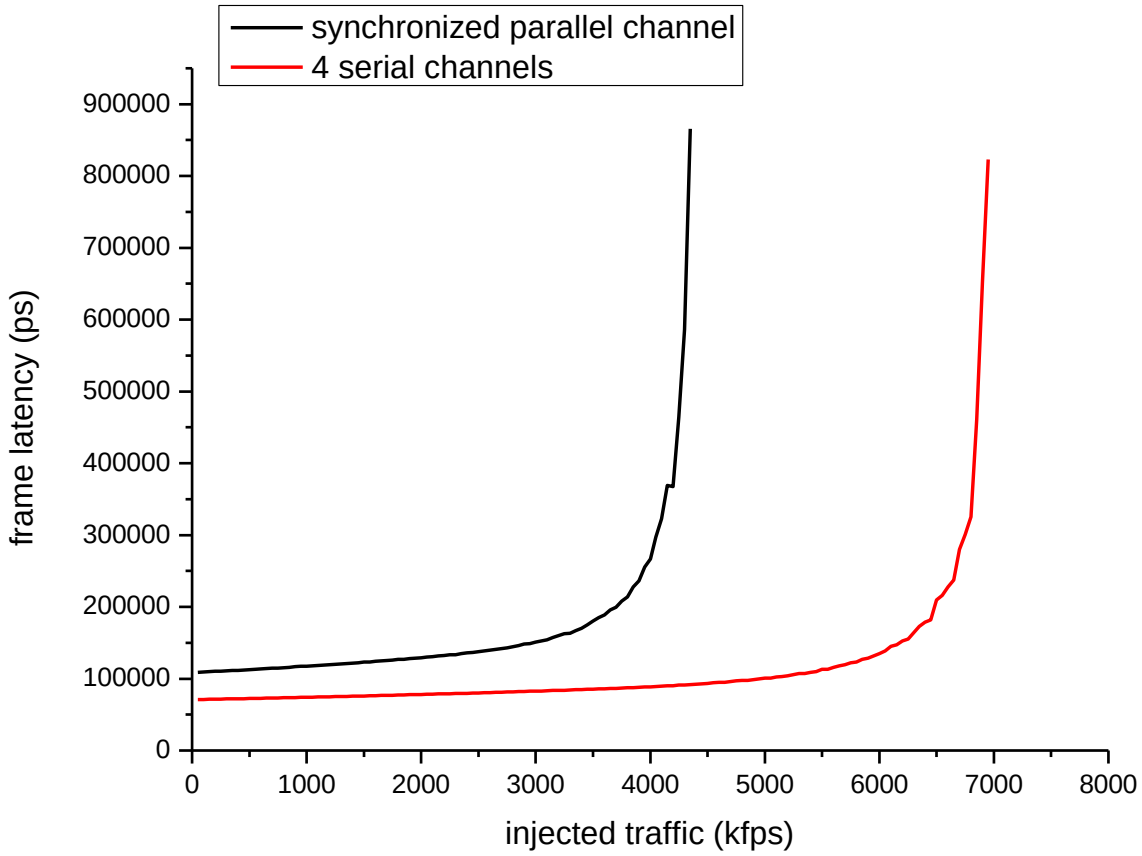
Router with serial channels



Frame Length 4-16 Bytes



Frame Length 96-128 Bytes



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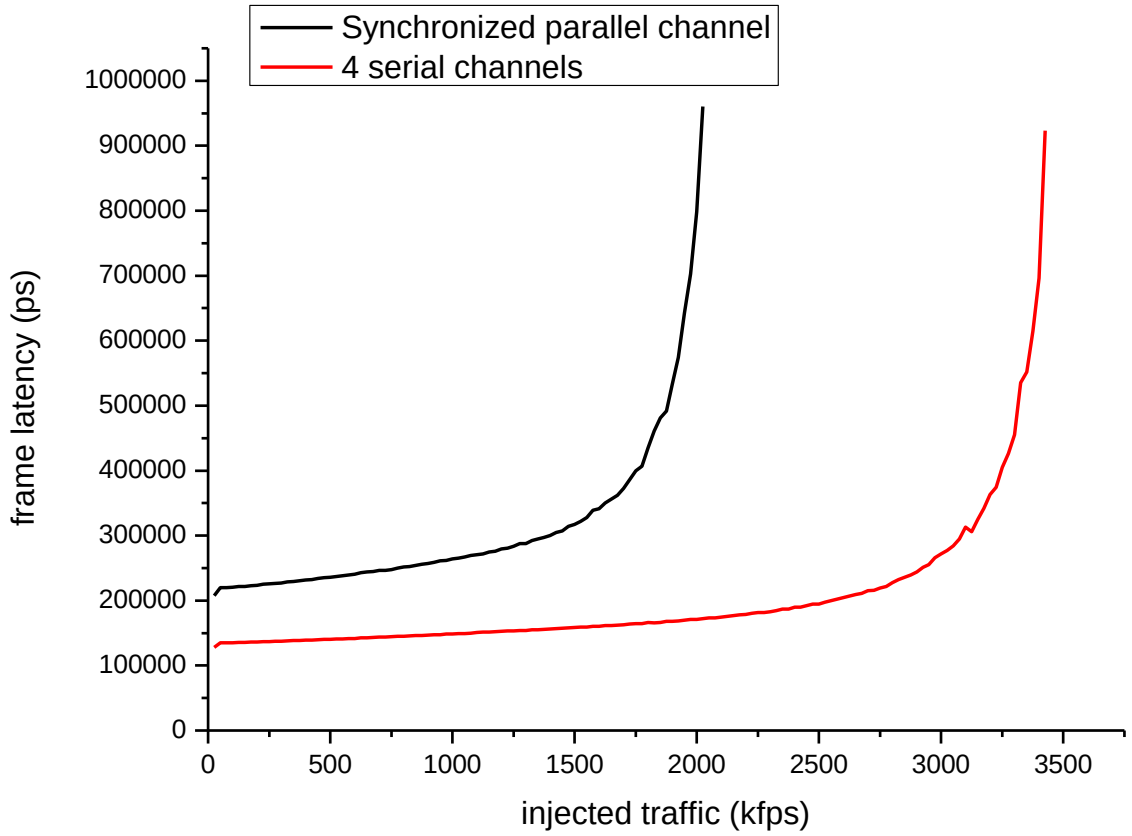
Frame Length 240-255 Bytes



Throughput with different frame lengths

	parallel	serial
4-16	0.25GByte	0.27GByte
96-128	0.50GByte	0.81GByte
240-255	0.45GByte	0.88GByte

Conclusion

- By constraining the number of request lines on each physical channel and separate the forward and backward channels, the DyLAR router is deadlock-free.
- Through realistic layout procedure, HSpice simulation, and NoC simulations, divide a parallel channel into several serial channel could improve throughput and reduce frame latency.