

Spatial Parallelism in Asynchronous On-Chip Routers

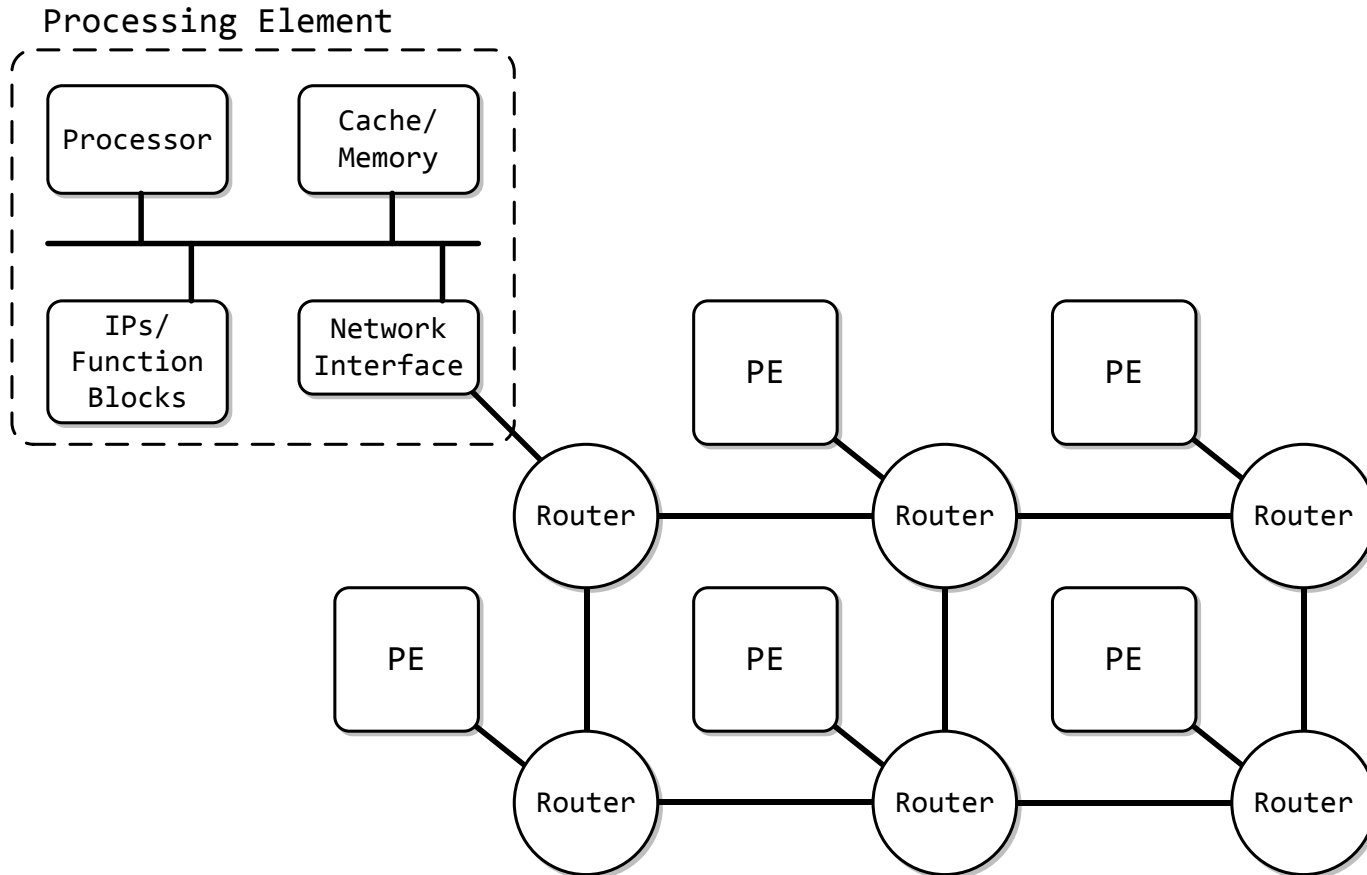
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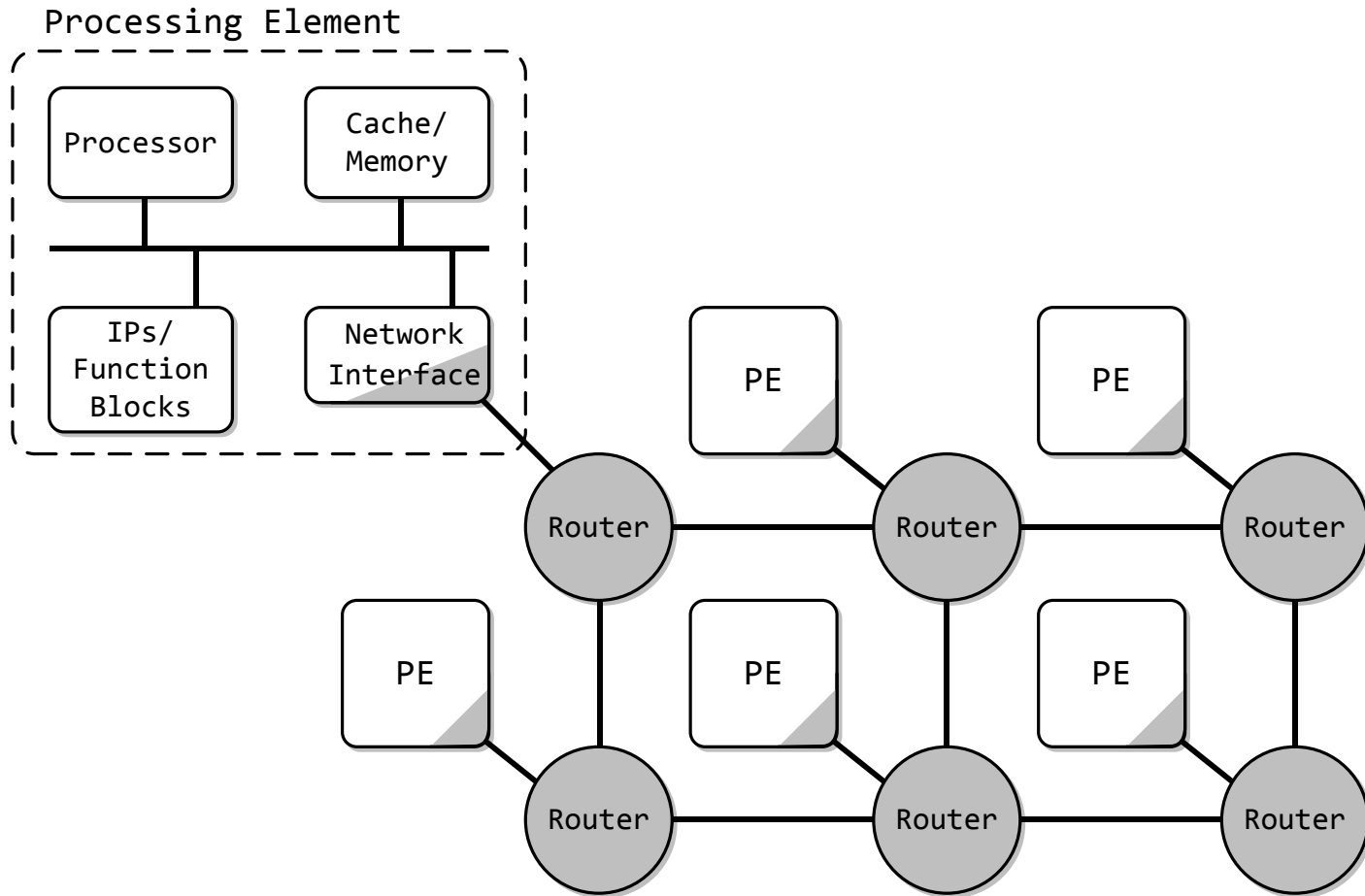
Content

- Introduction
- Techniques
 - Physical layer
 - Channel slicing
 - Switching layer
 - Spatial division multiplexing (SDM)
 - 2-stage Clos switch
- Asynchronous SDM router
- Conclusion

Network on Chip



Asynchronous NoC



Network Layers

- Routing layer
 - Routing algorithm, deadlock and livelock, uni-cast and multi-cast
- Switching layer
 - Flow control method, buffer allocation, switch allocation
- Physical layer
 - Channel/link, pipeline structure

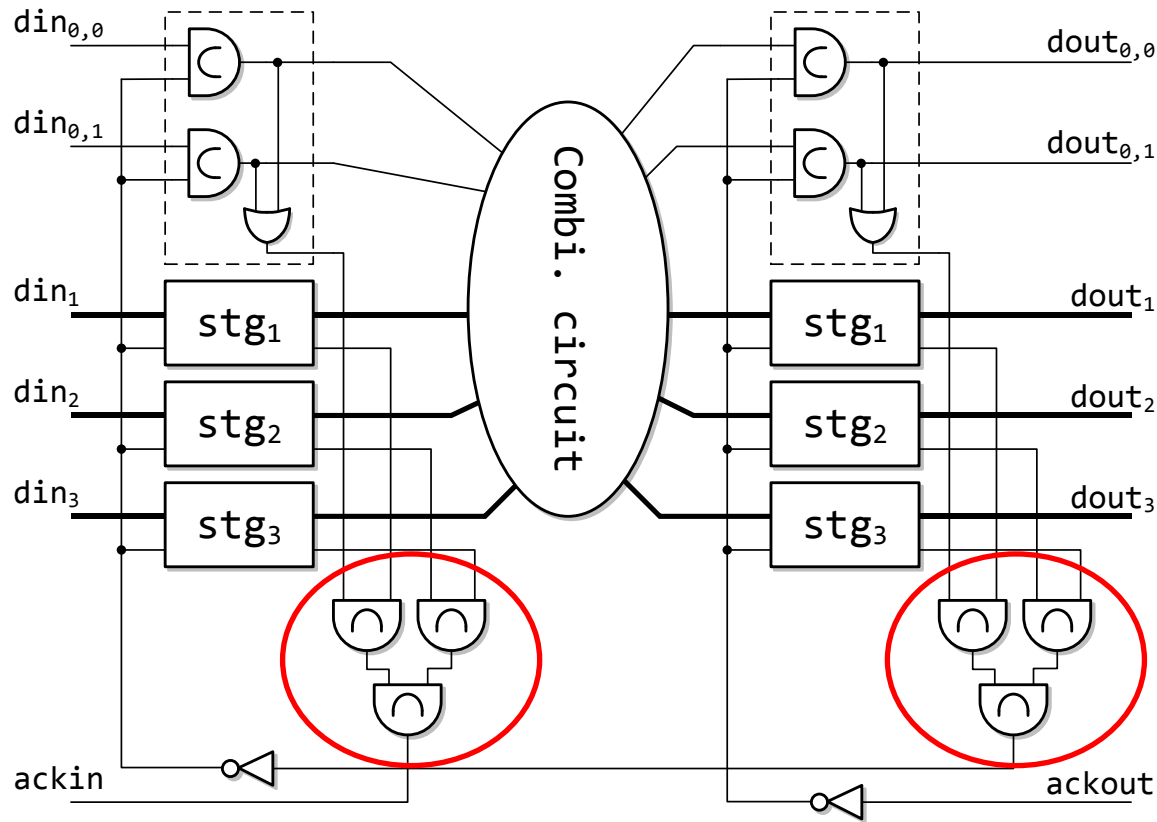
Research Objective

- To introduce spatial parallelism into physical and switching layers for high throughput.
- Physical layer
 - Channel slicing: removing synchroniztion
- Switching layer
 - Spatial division multiplexing
 - 2-stage Clos switch

Physical layer

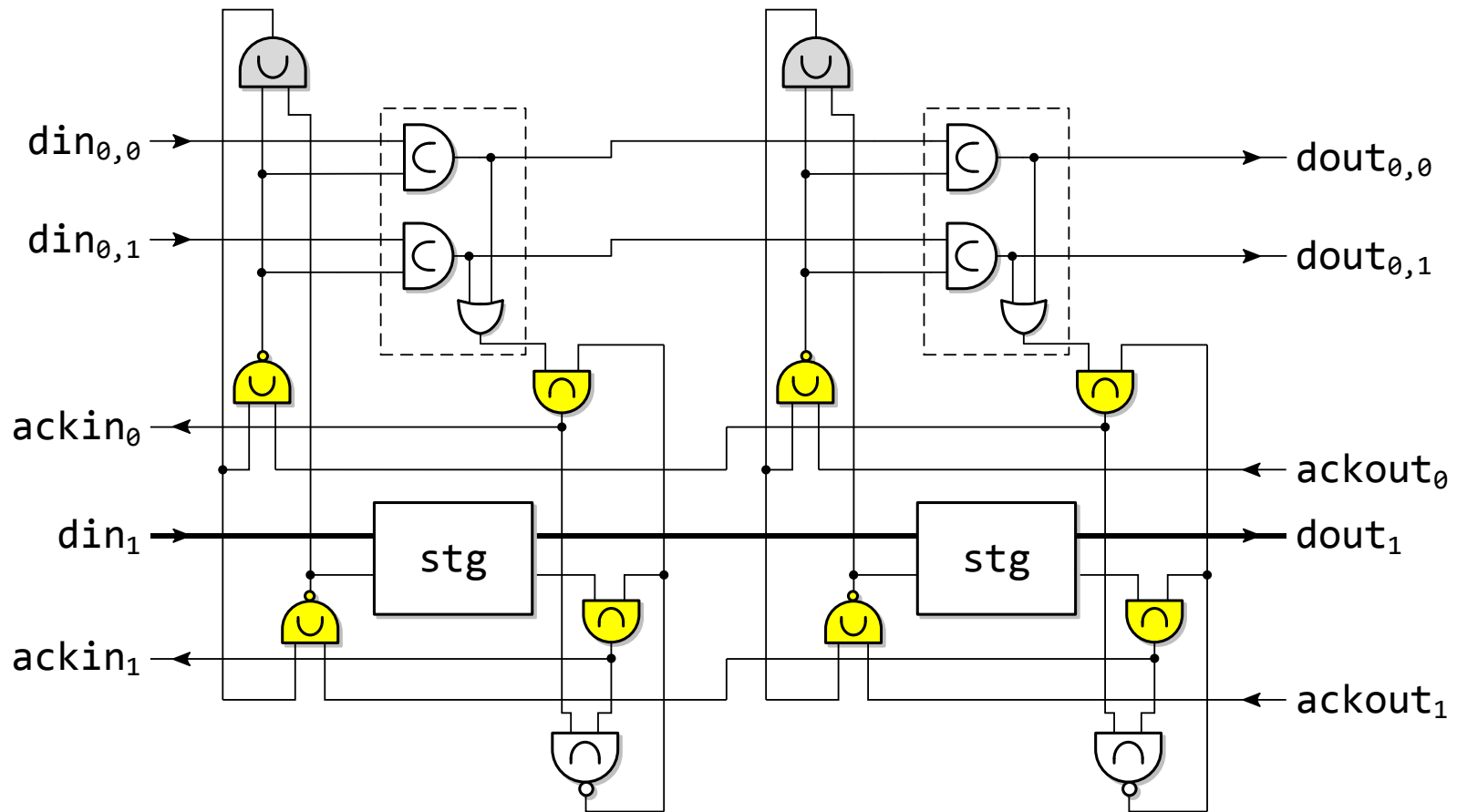
Pipeline styles

Synchronized Pipeline



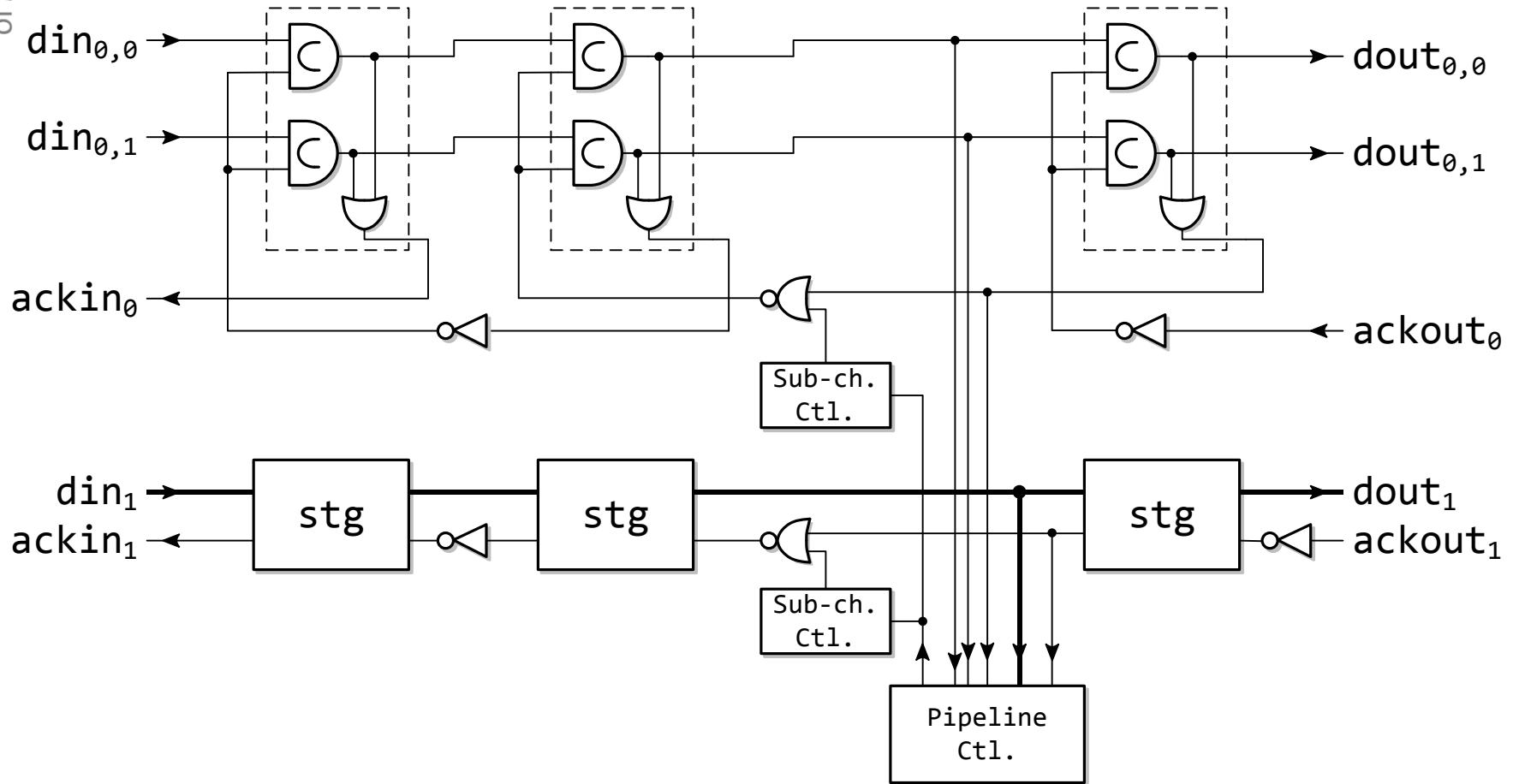
ANoC, QoS NoC, SpiNNaker, ASPIN

Pipelined Completion Process

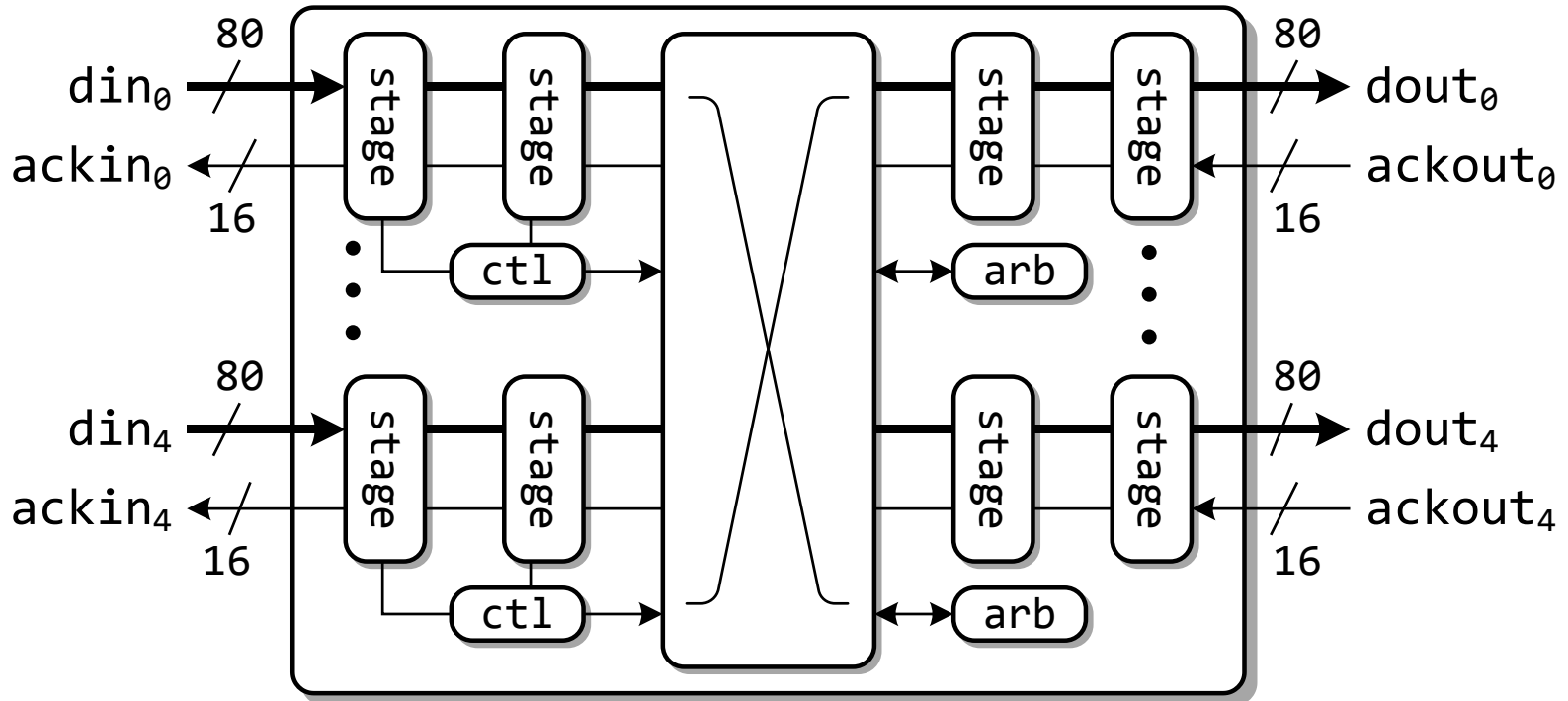


A. J. Martin, A. M. Lines, and U. V. Cummings. Asynchronous circuits with pipelined completion process, 2002. US patent 6,502,180

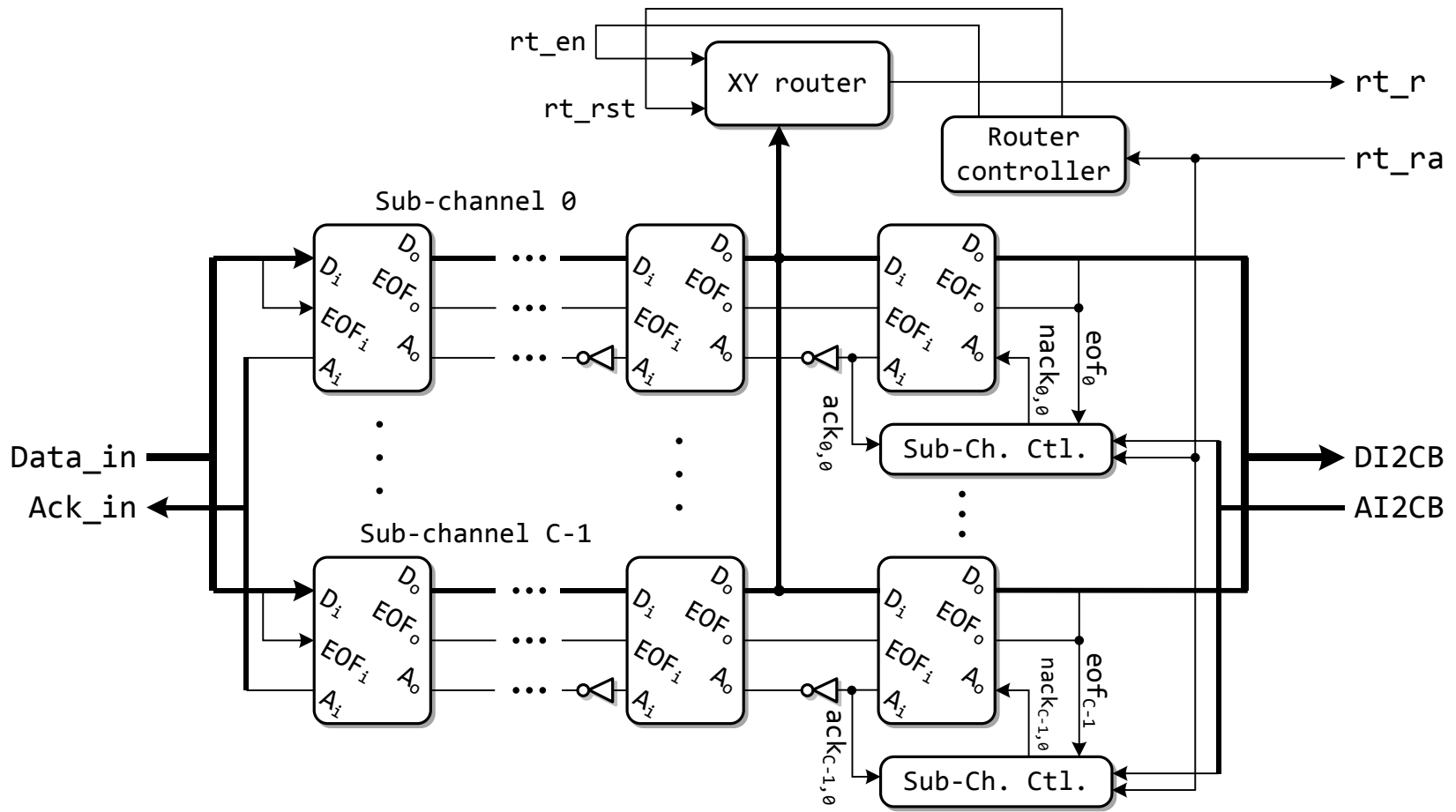
Channel Slicing



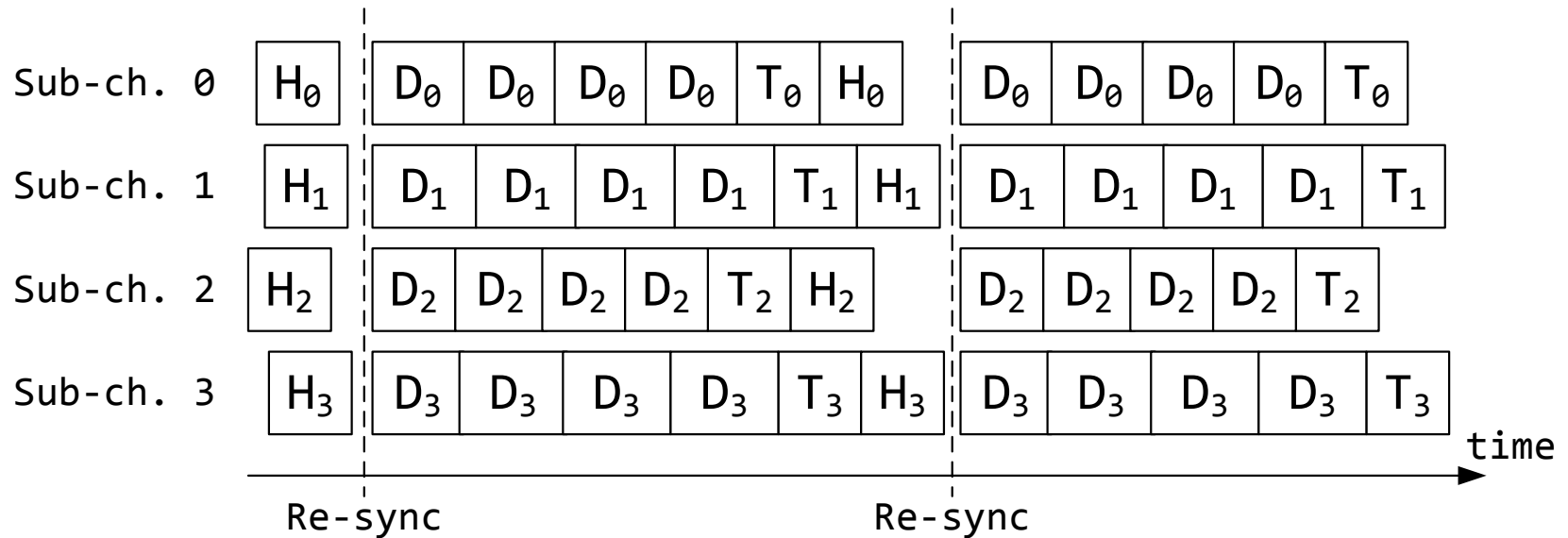
Using ChSlice in Routers



Using ChSlice in Routers



Data Flow using ChSlice



Wormhole Routers

Area

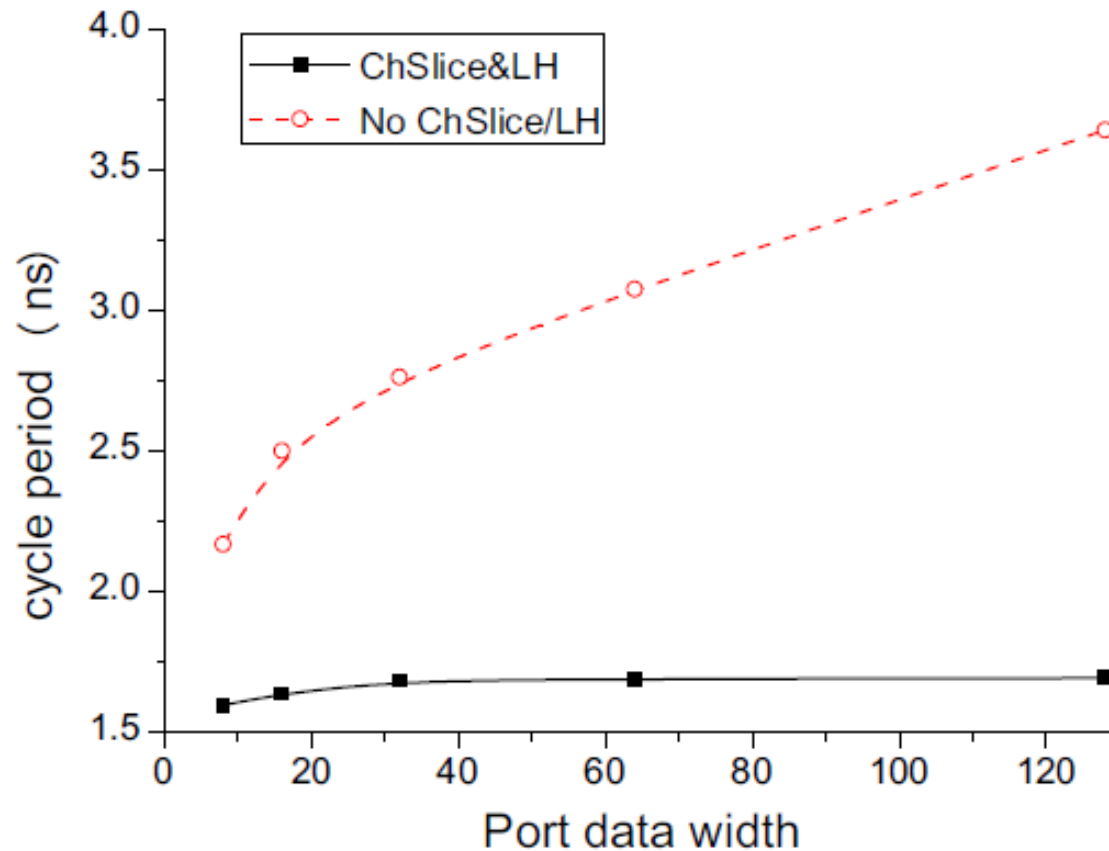
	Input Buffer	Output Buffer	Switch	Overall
Normal	4.3k	4.4k	2.3k	11.3k
ChSlice	5.8k	4.5k	3.2k	12.9k

Speed

	Cycle Period	Equ. Freq.	Latency	Routing
Normal	2.9ns	345MHz	2.8ns	0.8ns
ChSlice	2.2ns	455MHz	2.1ns	0.8ns

W. Song and D. Edwards. A low latency wormhole router for asynchronous on-chip networks. In Proc. of Asia and South Pacific Design Automation Conference, pages 437–443, 2010.

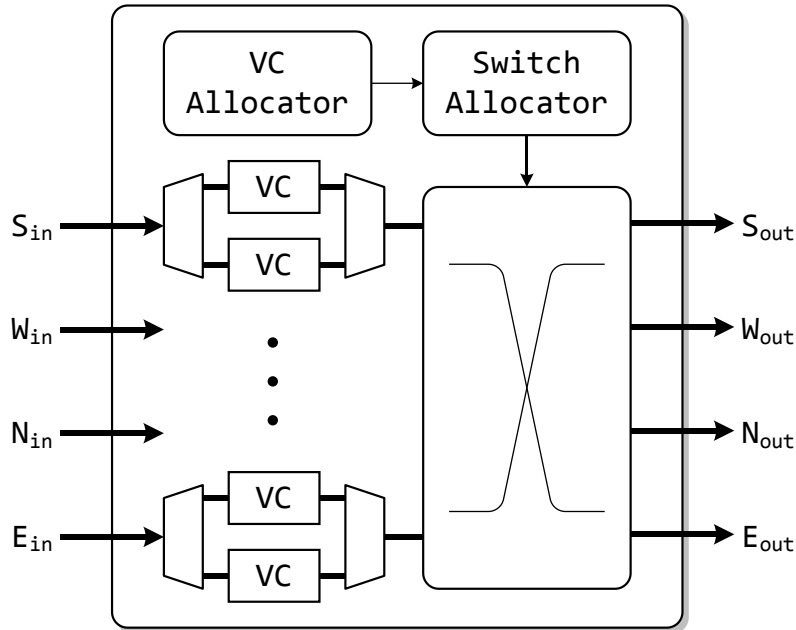
Data Width Effect



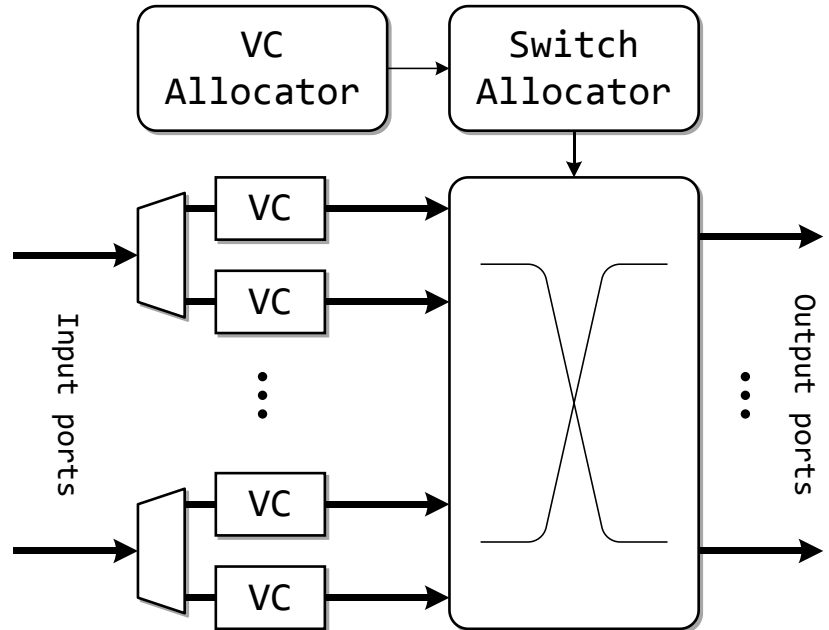
Switching Layer

Flow control method

Virtual Channel

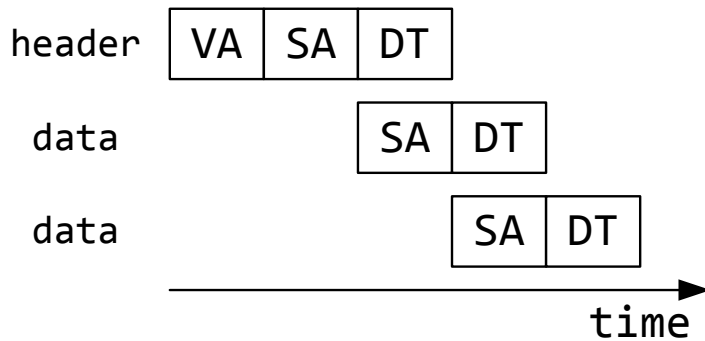


QoS NoC

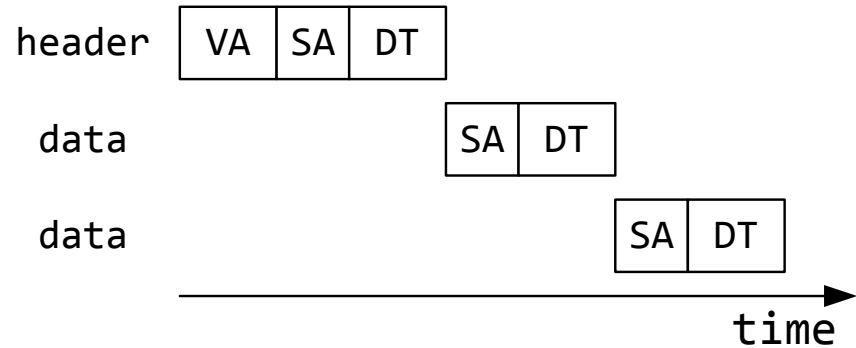


ANoC, QNoC, MANGO

Synchronization in Async VC



Synchronous VC router



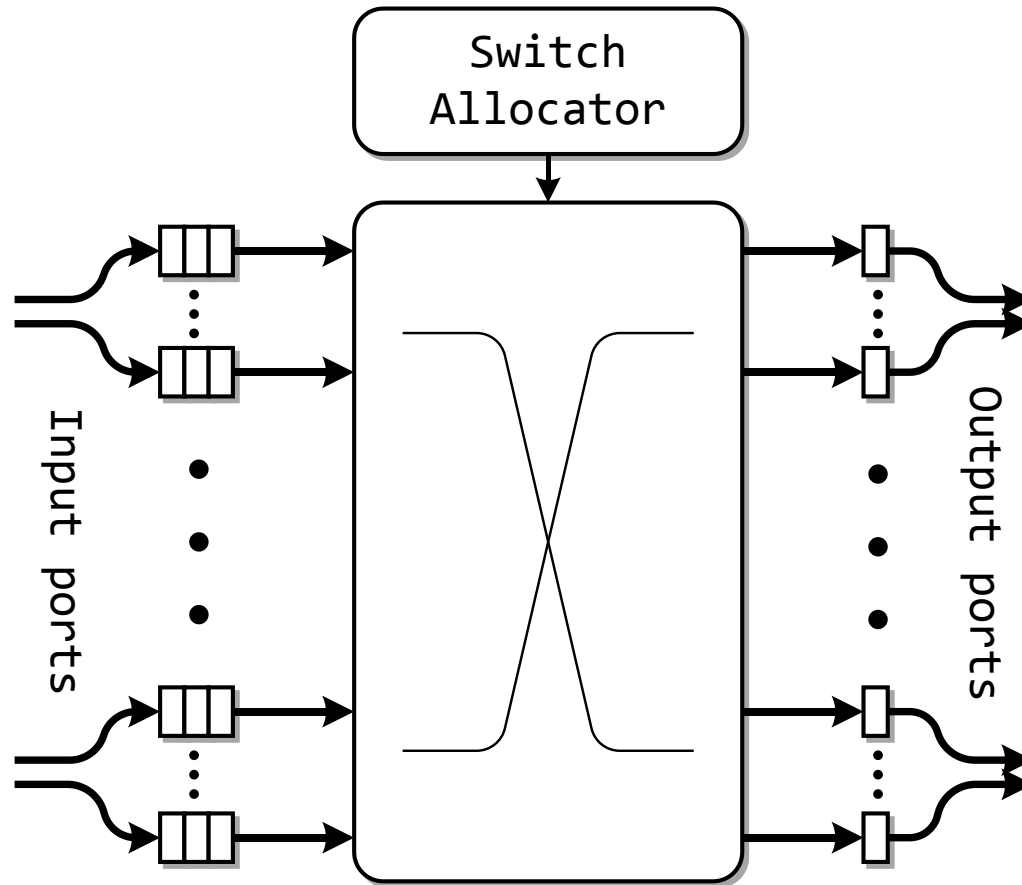
Asynchronous VC router

The central switch cannot be allocated in a pipelined way.

Design Overhead of VC

- Speed
 - The extra switch allocation latency.
 - Channel Slicing cannot be used.
- Area
 - Duplicated input buffers and the enlarged central switch plus an extra VC allocator.
 - The minimal buffer depth is 3
 - 1 full stage (2 stages) + 1 bubble stage

Spatial Division Multiplexing



Compare with VC

- VC
 - Extra switch allocation latency in each flit
 - No ChSlice
 - Credit loop constraint
 - Duplicated buffer and control
 - Increased crossbar
 - Extra VC allocator
- SDM
 - Extra switch allocation latency in each frame
 - Can use ChSlice
 - Serialized frame
 - Same buffer with extra control
 - Increased crossbar
 - Enlarged SW allocator

SDM routers

Area (μm^2)

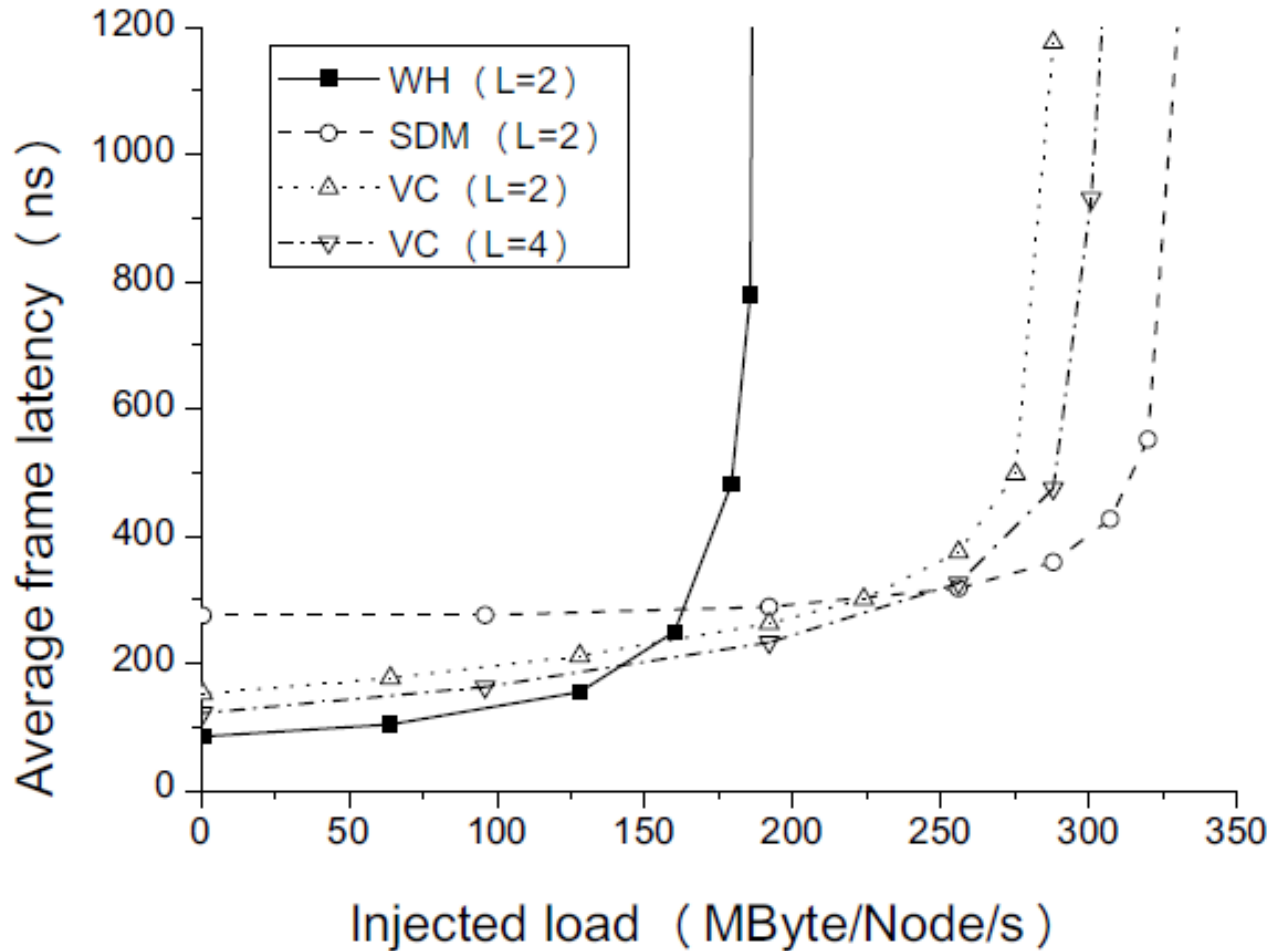
	Input Buffer	Output Buffer	Crossbar	Switch Allocator	Total
Wormhole	14,303	5,935	4,356	772	25,366
SDM	21,995	6,000	21,744	22,208	71,956

Speed (ns)

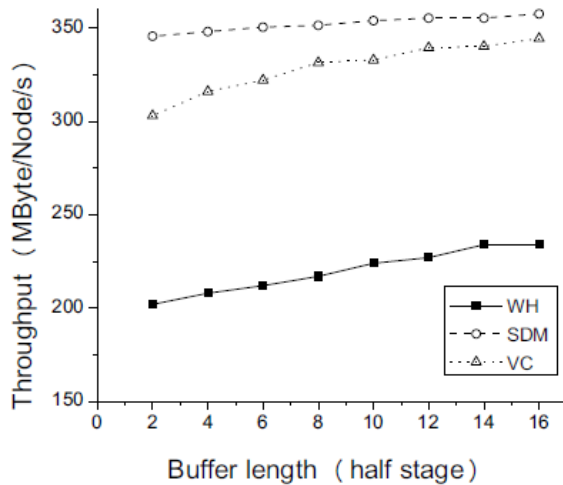
	Cycle	Latency	Routing	Allocator
Wormhole	4.22	2.29	0.44	0.78
SDM	4.10	2.49	0.51	3.21

W. Song and D. Edwards. Asynchronous spatial division multiplexing router. *Microprocessors and Microsystems*, 35(2):85–97, 2011.

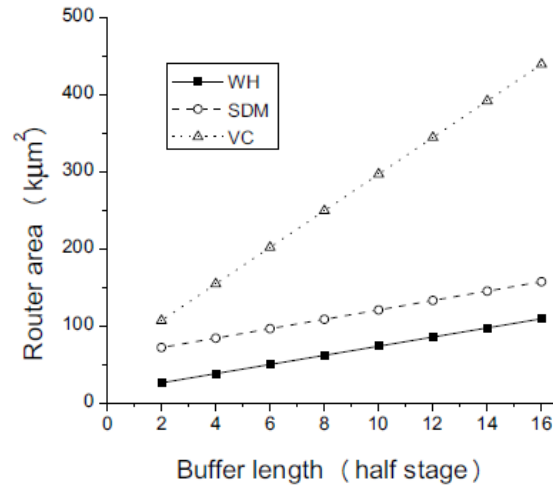
Basic Performance



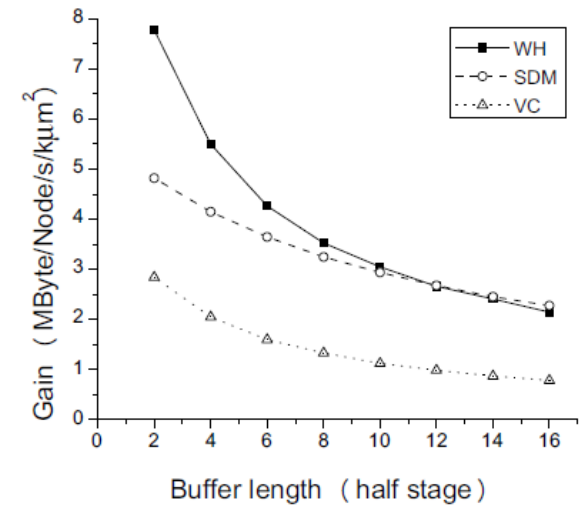
Buffer Size



(a) Throughput

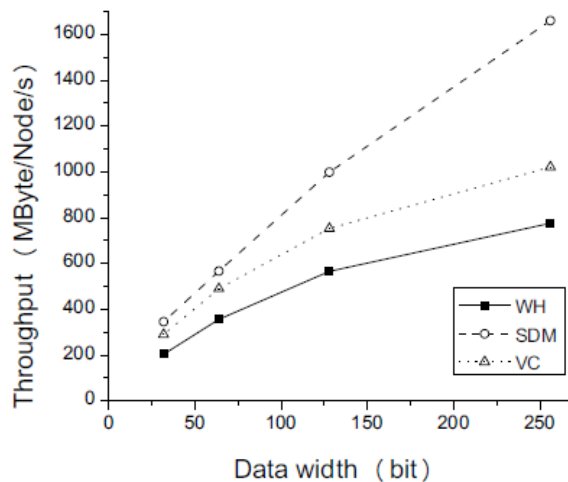


(b) Area

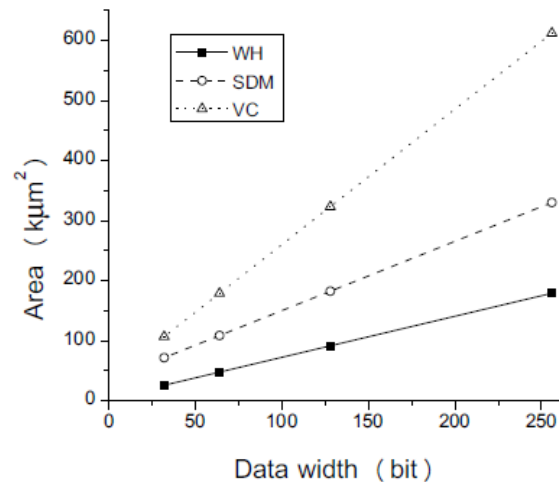


(c) Gain

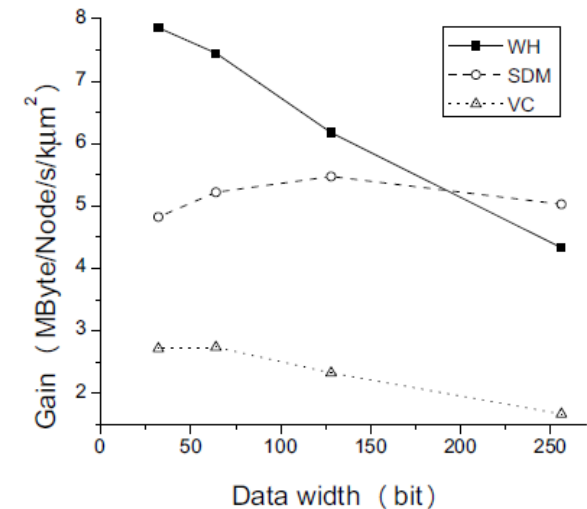
Data Width



(a) Throughput



(b) Area

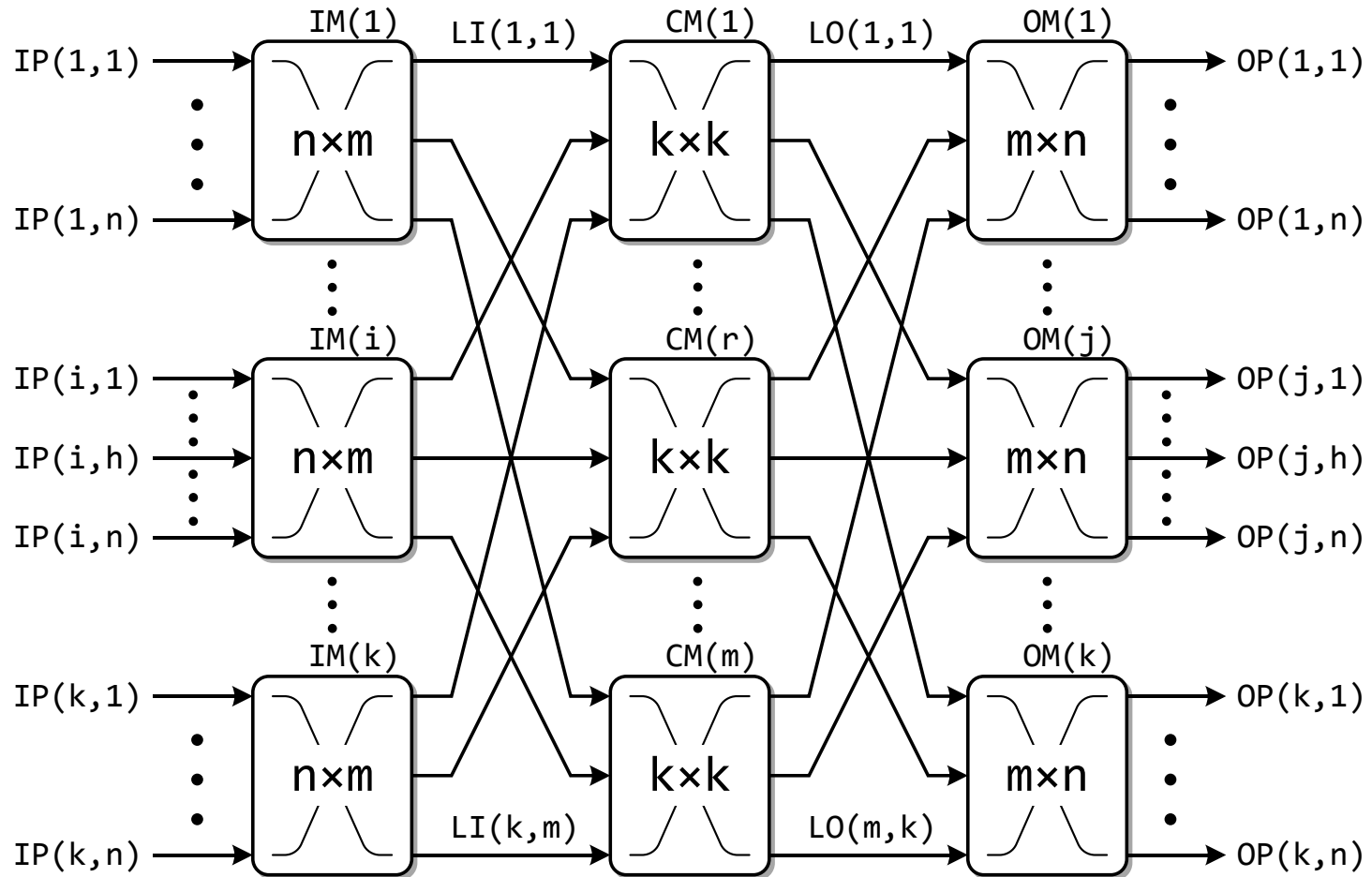


(c) Gain

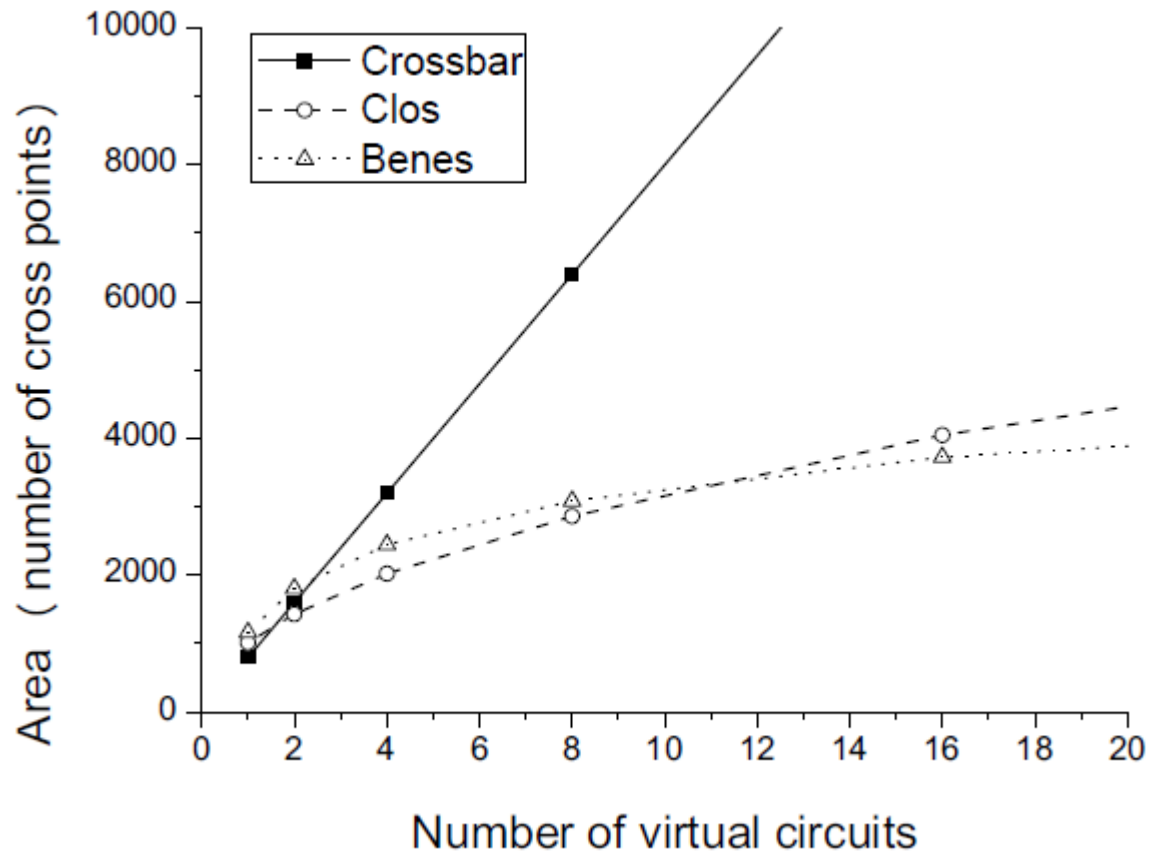
2-Stage Clos Network

Reduce the area overhead of SDM

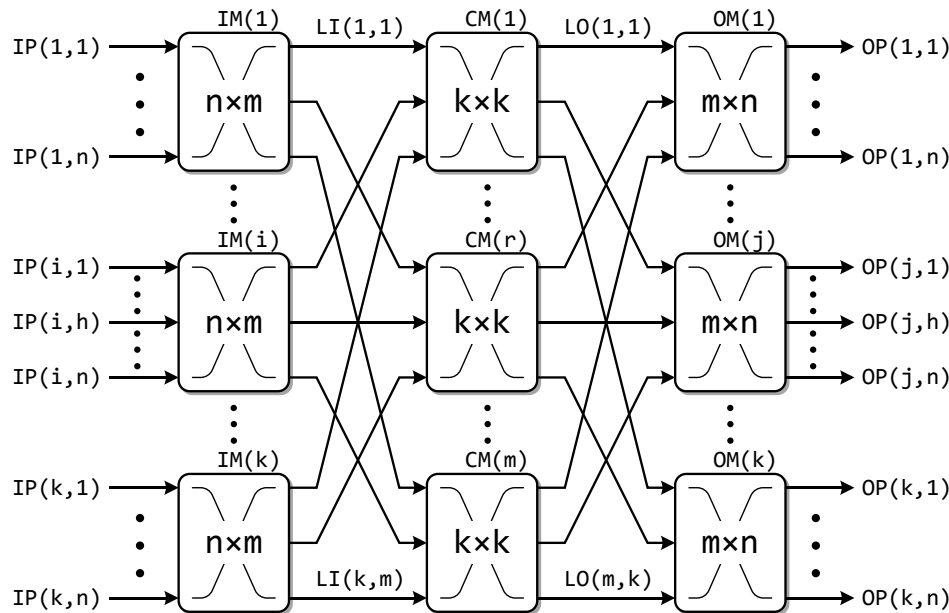
What is Clos



Area Consumption

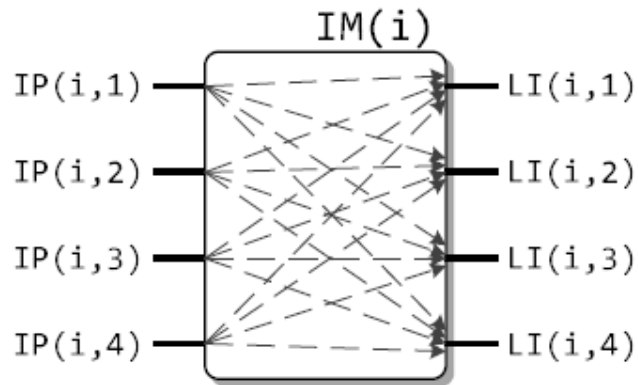


Concurrent Round-Robin Dispatching

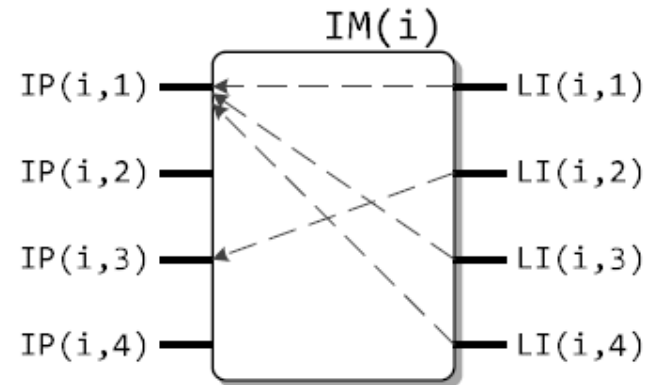


- Match with in IMs
Parallel iterative matching (PIM)
- Match within CMs
Random
- Match within OMs
Random

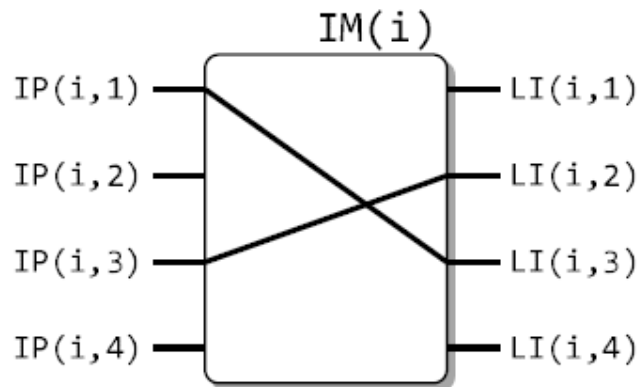
Parallel Iterative Matching



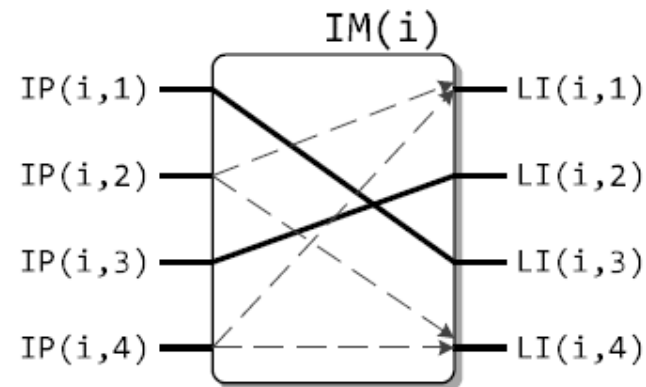
(a) Step 1, request



(b) Step 2, grant

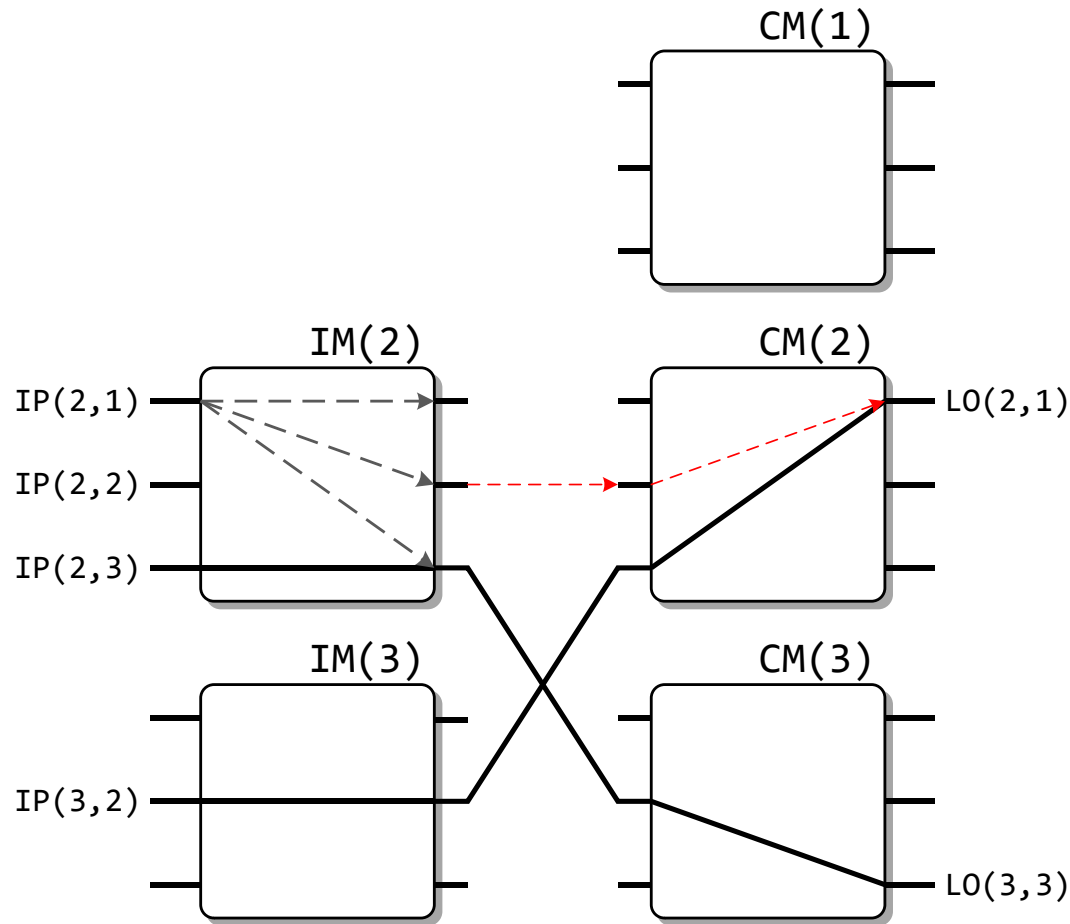


(c) Step 3, accept



(d) Step 1, next iteration

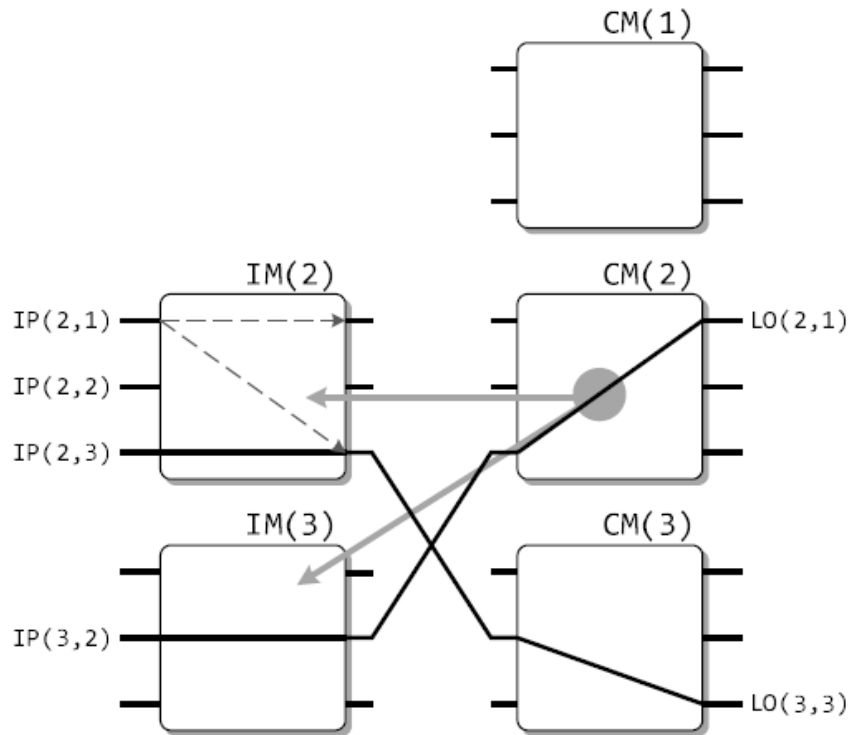
Contention in CMs



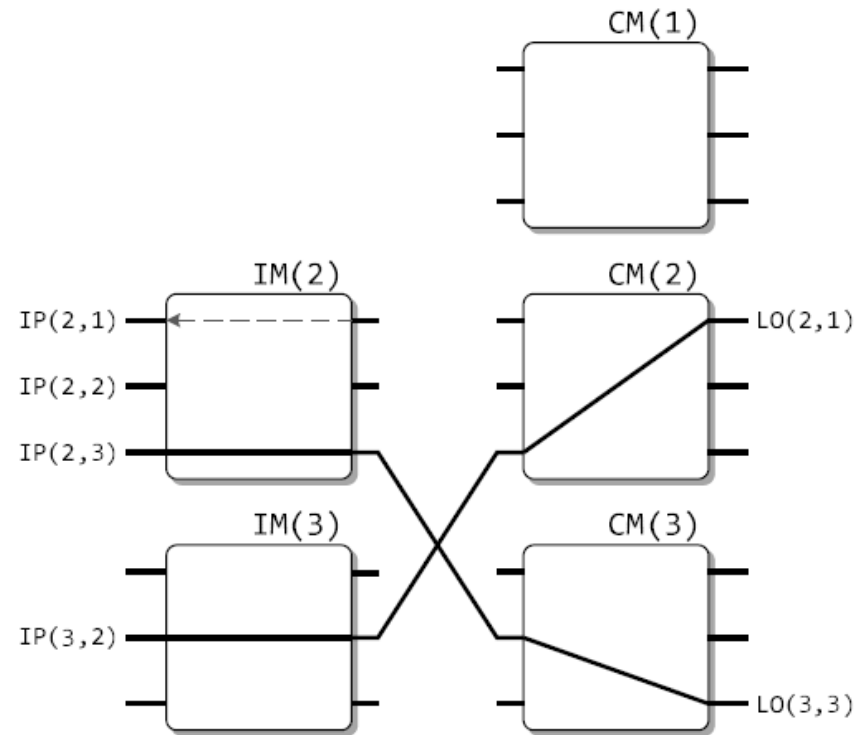
Issues of Async Dispatching

- No clock and no synchronization
 - Frames arrive asynchronously
 - All circuits are event-triggered
 - CM contention can cause large latency

Async Dispatching

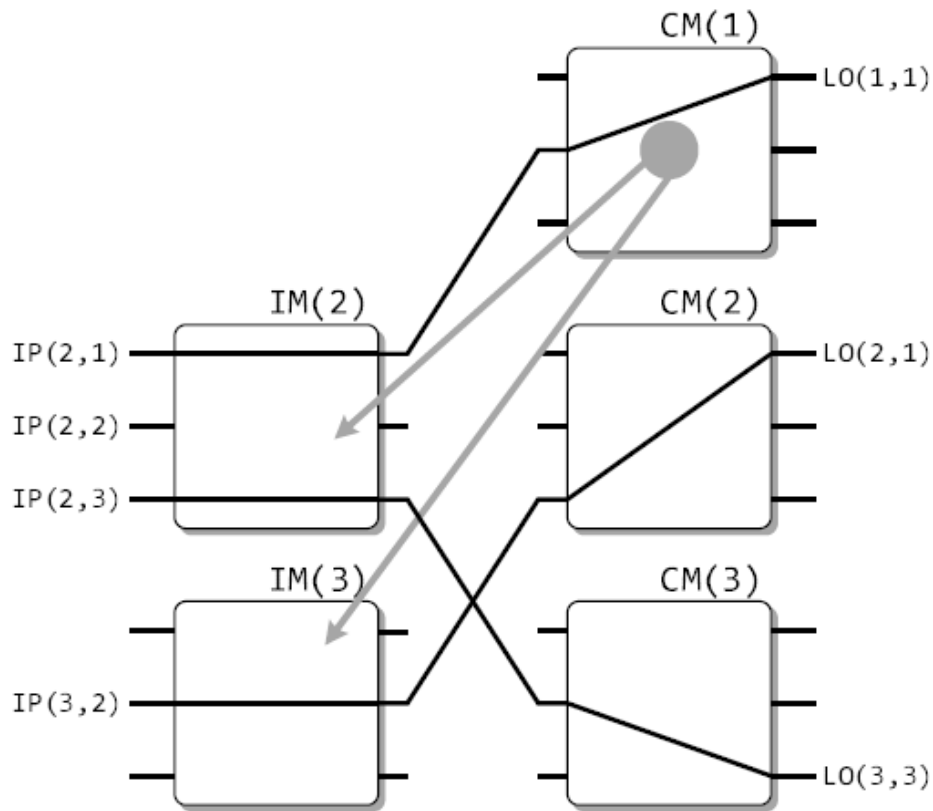


(a) IP requests



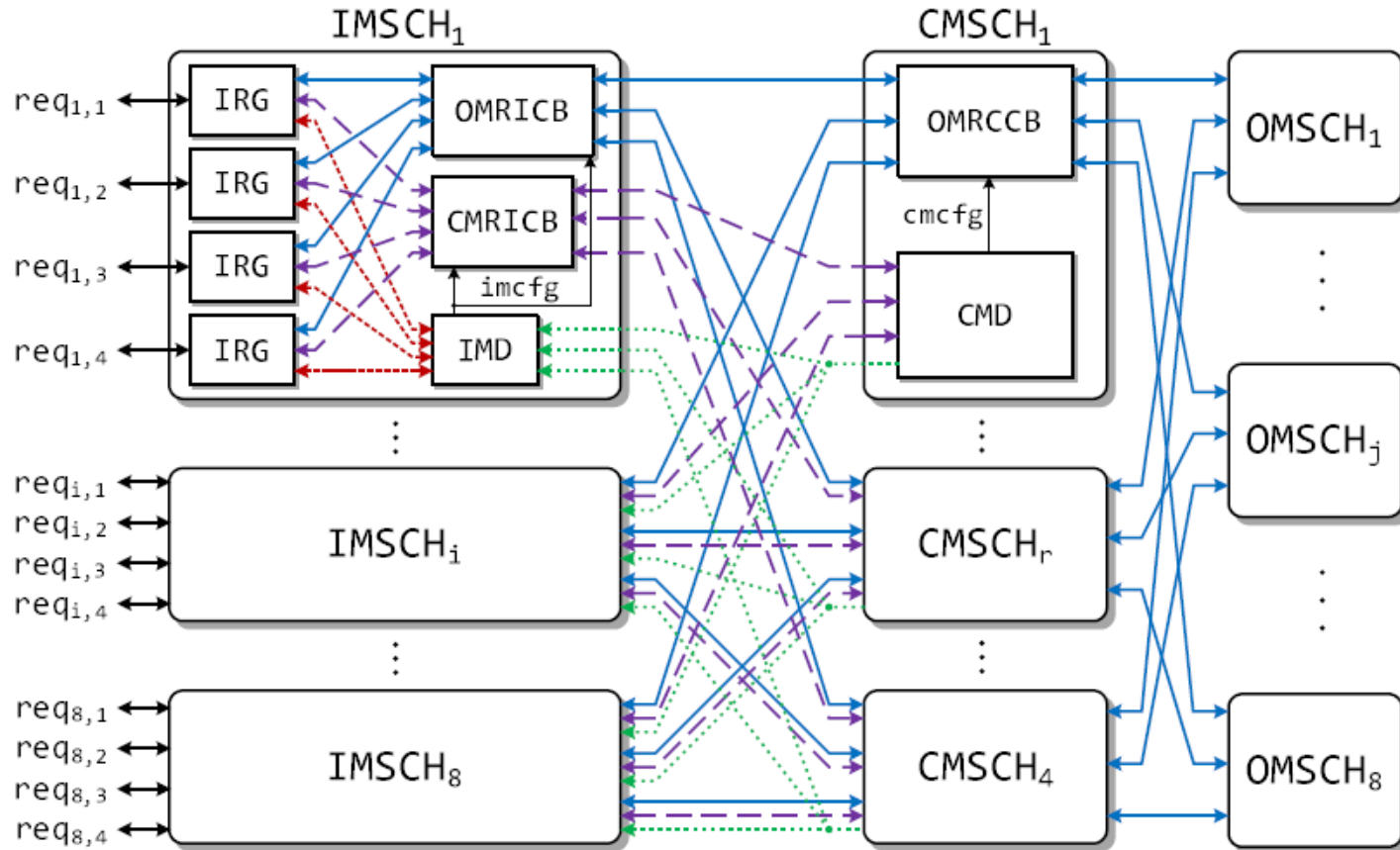
(b) Grant return

Async Dispatching



(c) State feedback

Async Clos Scheduler



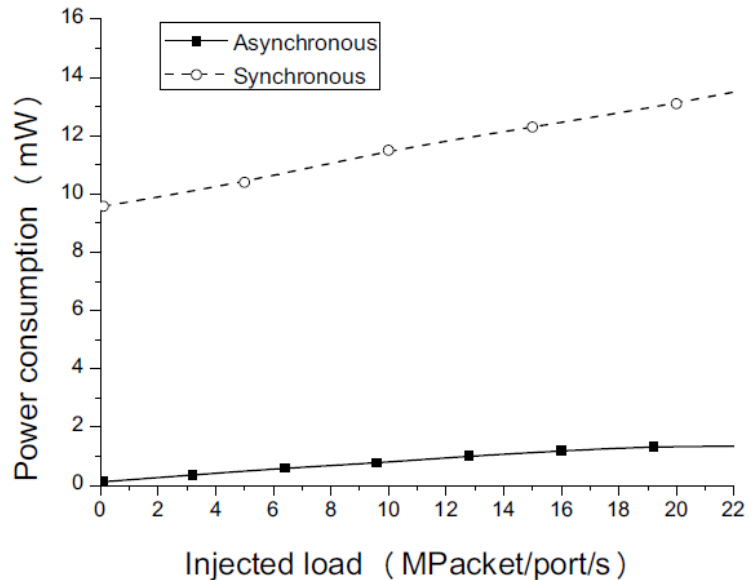
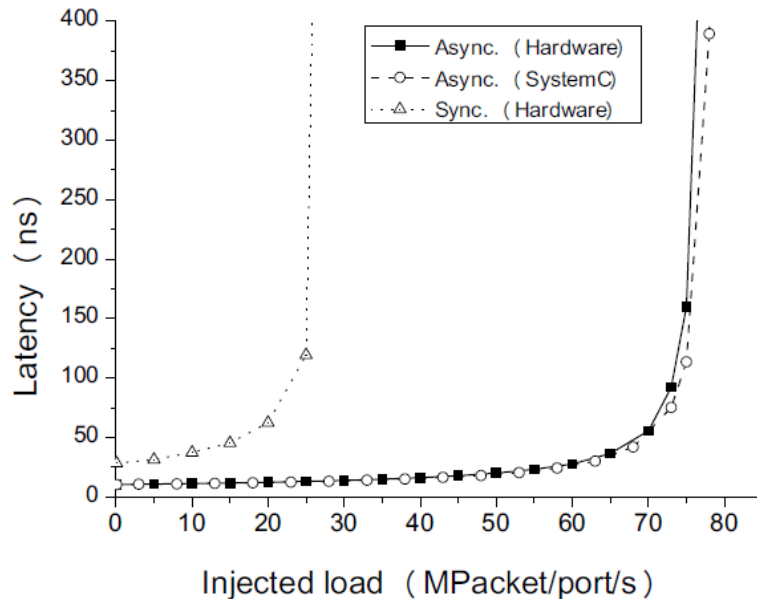
W. Song and D. Edwards. An asynchronous routing algorithm for Clos networks. In Proc. of International Conference on Application of Concurrency to System Design, pages 67–76, 2010.

Sync/Async Comparison

	IMD	CMD	OMSCH	IRG	Total
Async	3,862	4,879	985	160	88,057
Sync	3,186	6,498	1,375	0	115,262

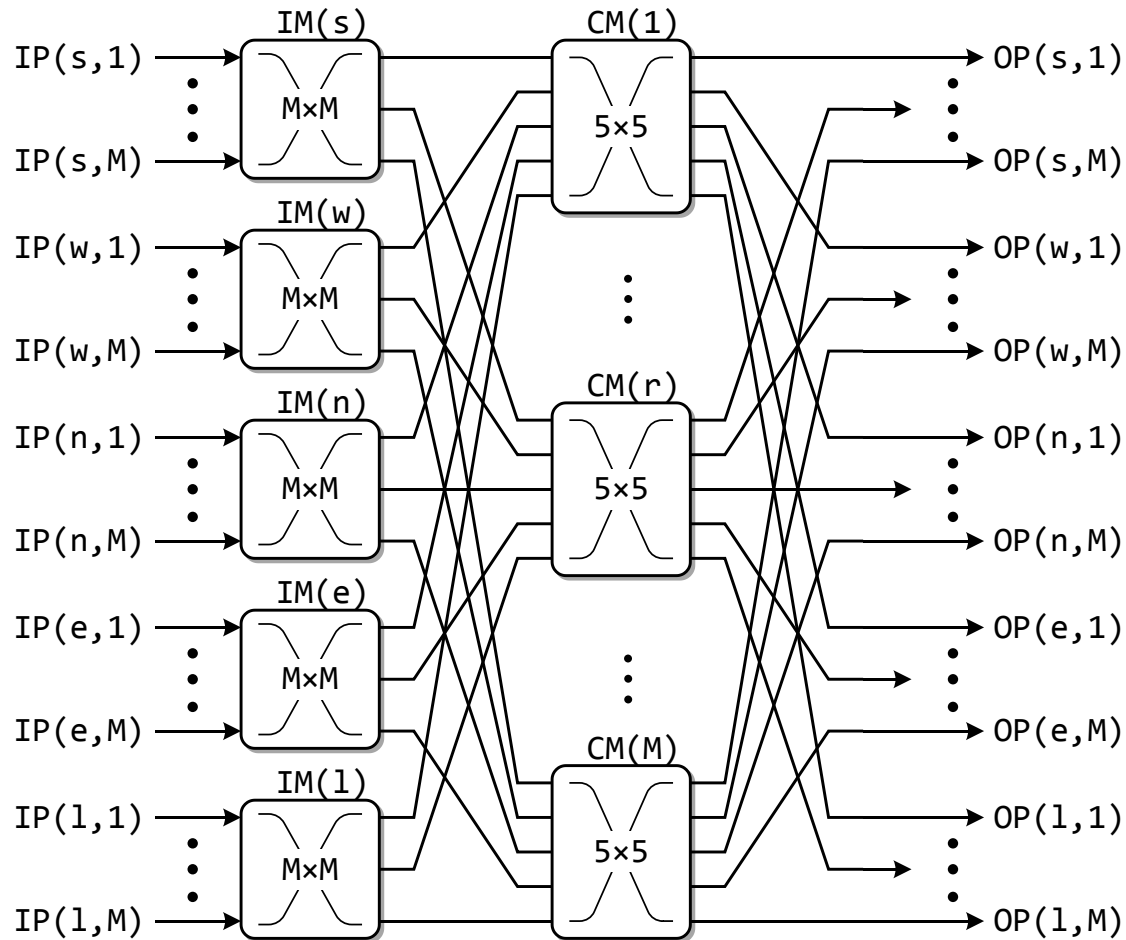
32-port 3-stage Clos with 8 CMs

Sync/Async Comparison

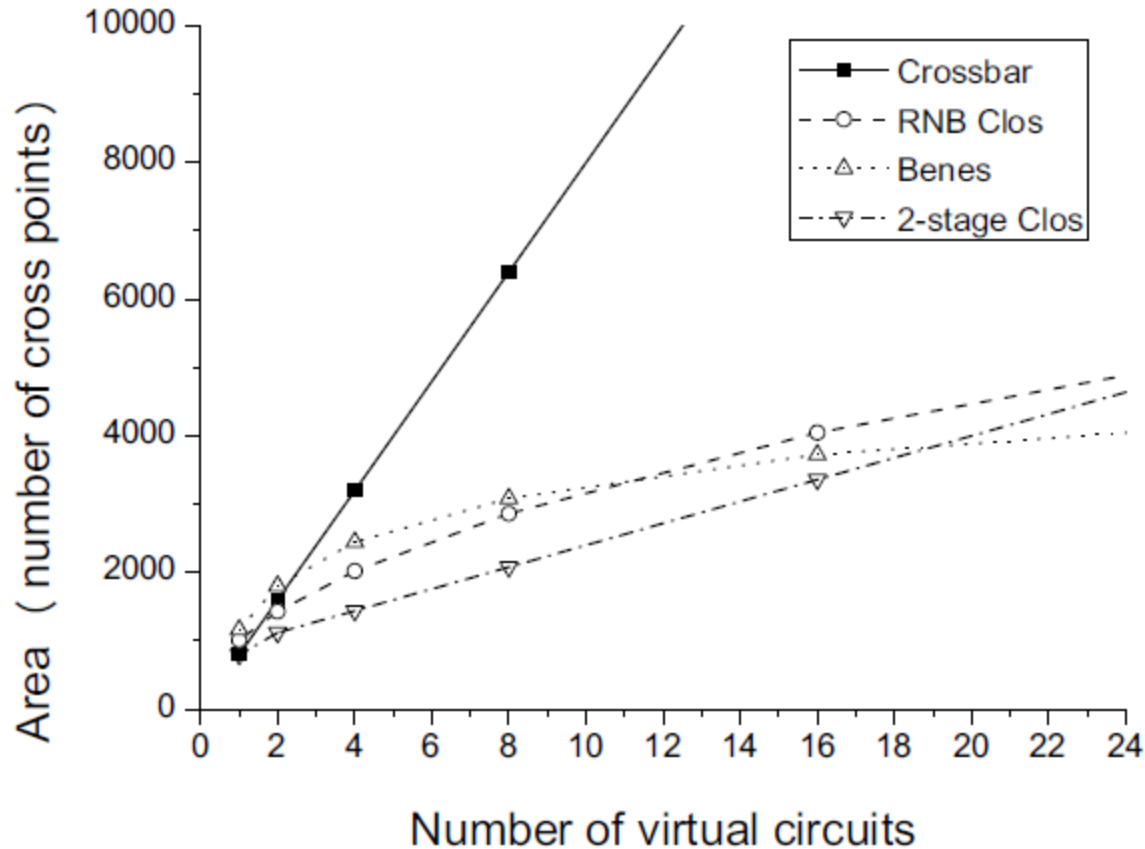


Sync: 285MHz, Clock tree 8.34 mW, 180 μ J/MPacket
Async: 64.4 μ J/MPacket

2-stage Clos Switch



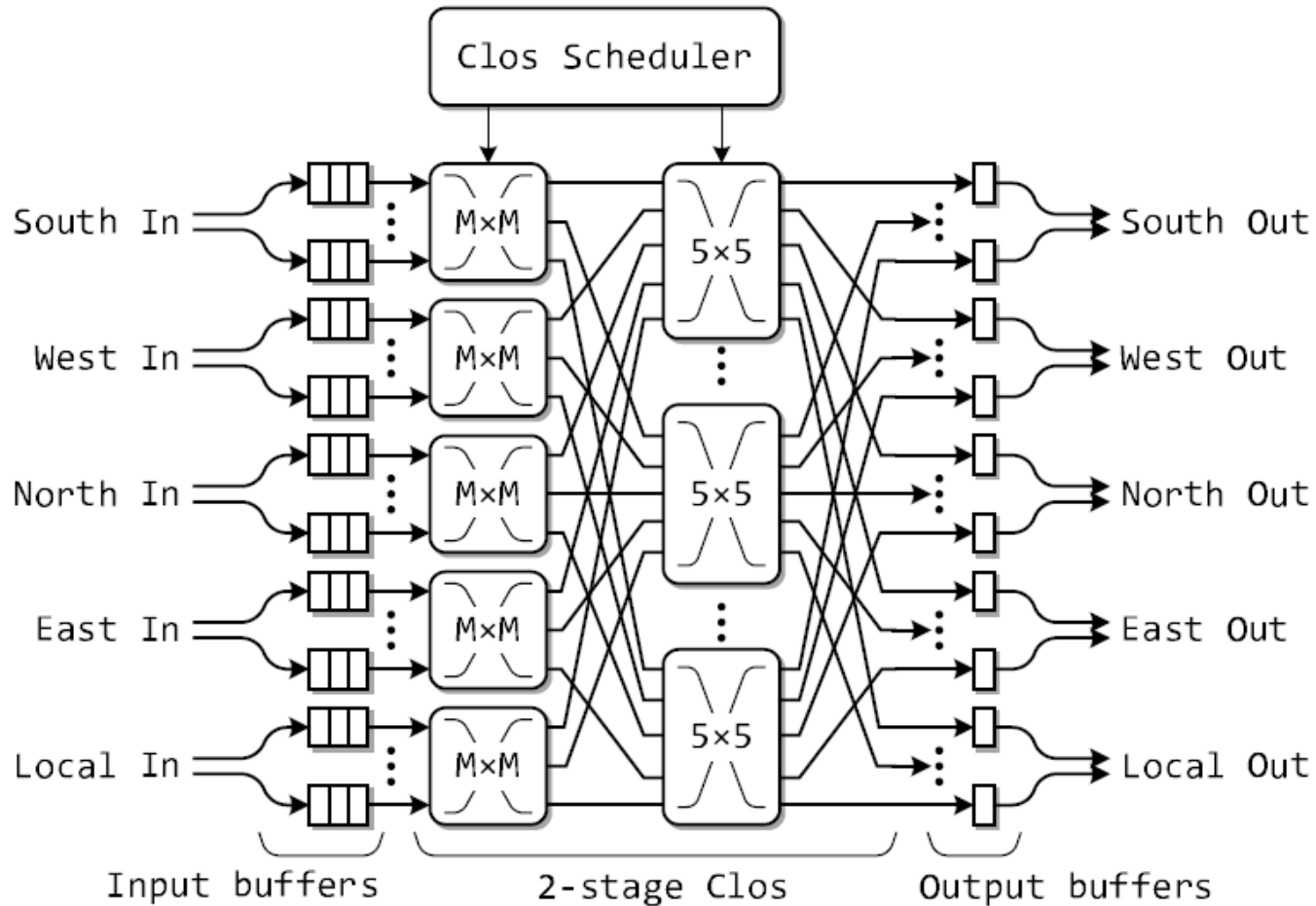
2-stage Clos Switch



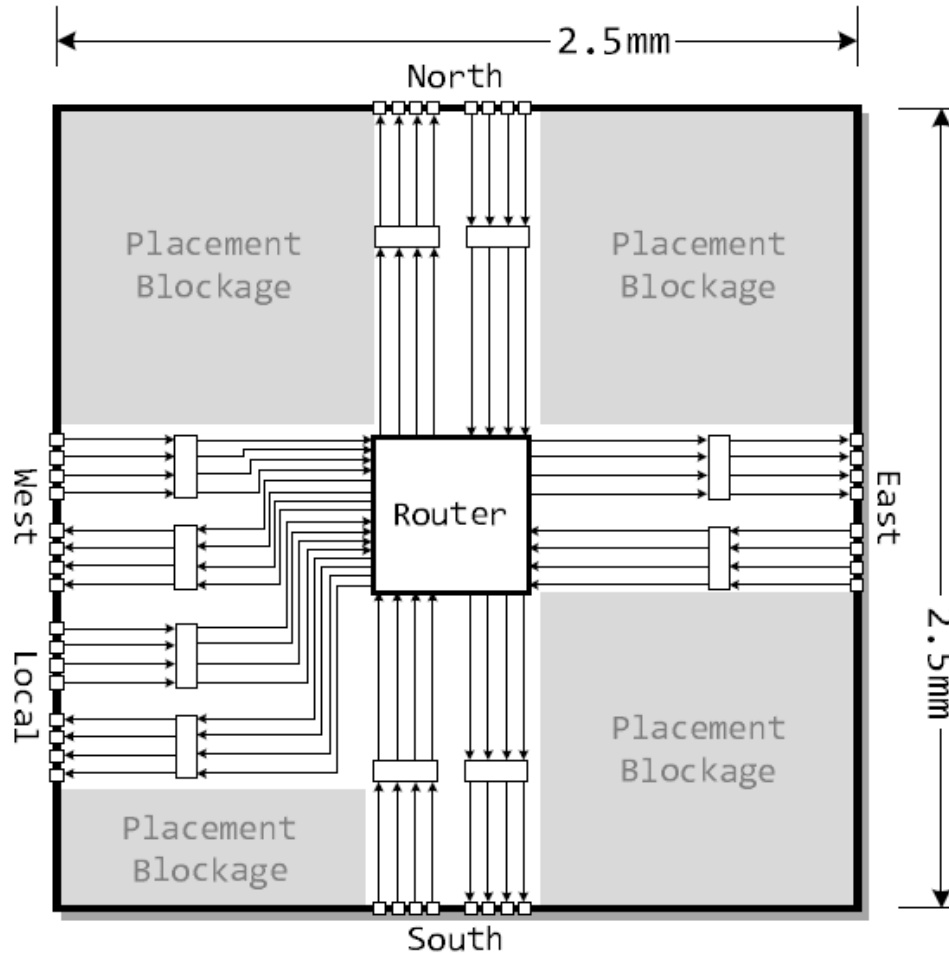
Asynchronous SDM Router

Put all together

Router Structure



Floorplan



Faraday 0.13 μm
Standard cell lib

Single Router

Area 32-bit 4VC μm^2

	Input Buffer	Output Buffer	Switch	SW Alloc	Total
WH	8,827	8,120	8,995	909	27,271
WH+ChSlice	17,147	11,034	17,754	909	48,170
SDM	18,580	9,443	47,485	34,823	111,343
SDM+ChSlice	23,032	8,927	65,300	34,965	134,534
SDM+Clos+ChSlice	19,995	8,893	33,417	19,884	84,054
VC	134,373	17,839	73,037	55,393	281,646

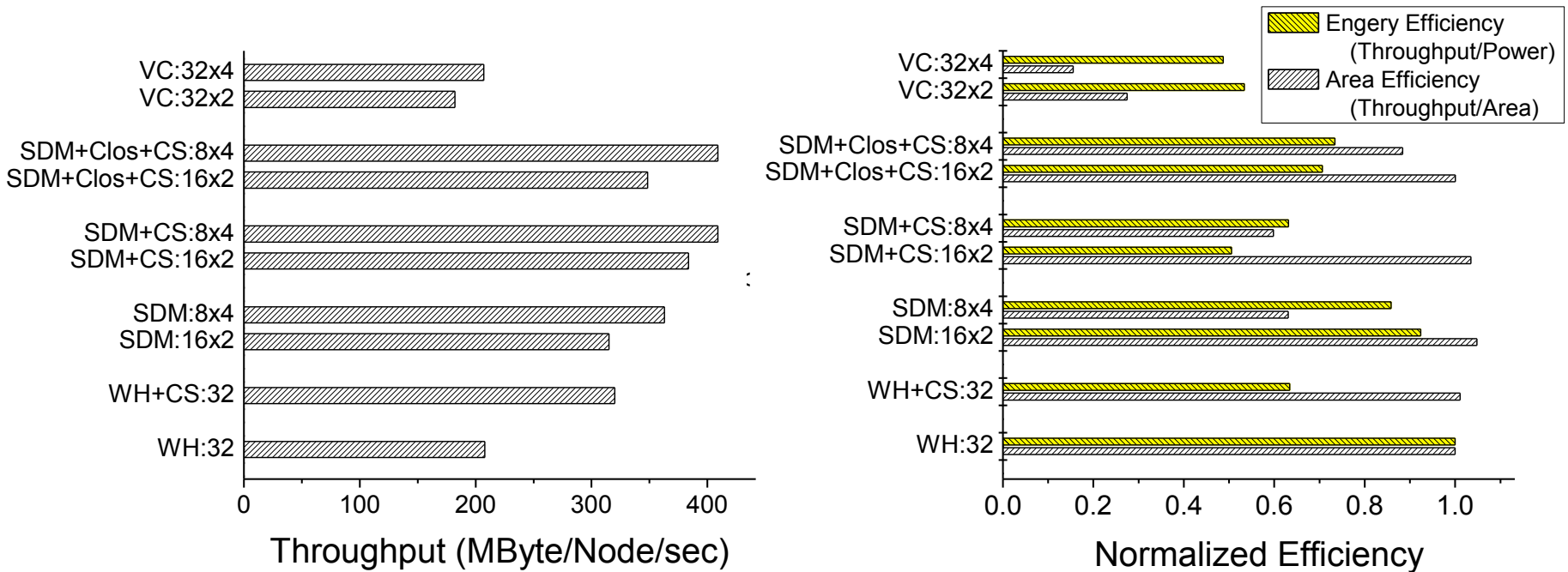
Single Router

Speed ns

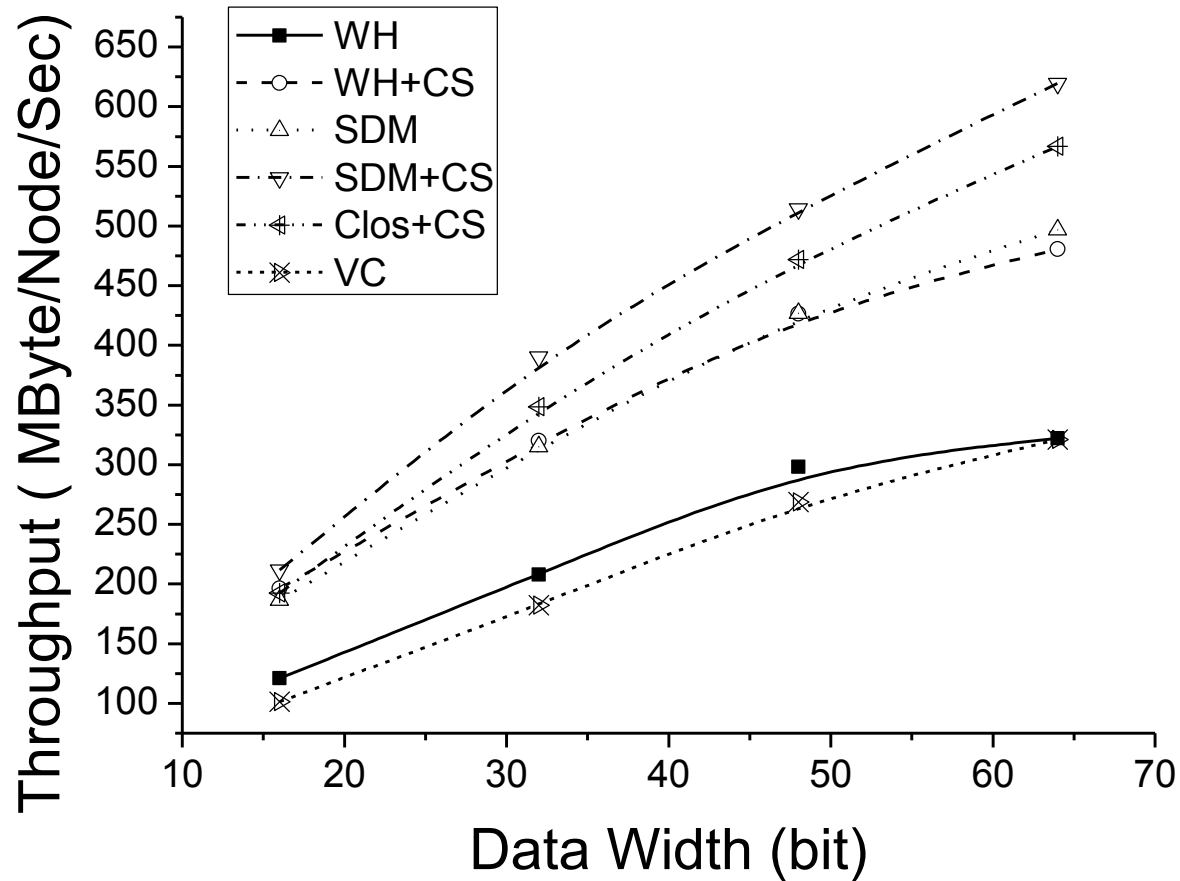
	Cycle	Equ. Freq.	Latency	Routing	Alloc.
WH	3.68	272MHz	0.96	0.61	1.06
WH+ChSlice	2.24	446MHz	0.92	0.64	1.24
SDM	3.27	306MHz	1.29	0.68	2.09
SDM+ChSlice	2.86	350MHz	1.18	0.68	2.01
SDM+Clos+ChSlice	2.67	375MHz	1.29	0.63	2.13
VC	6.93	144MHz	7.53	1.98	2.46

Different VCs

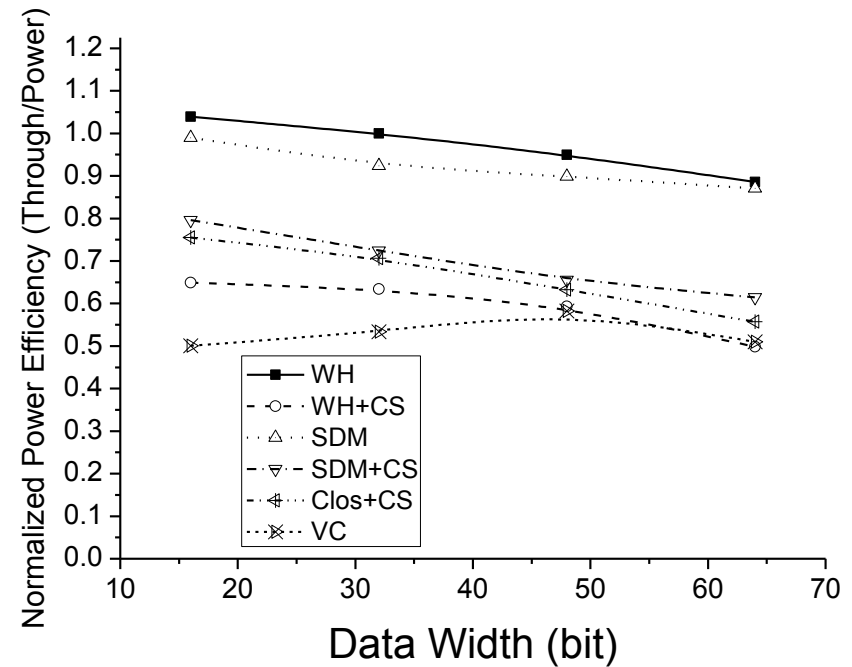
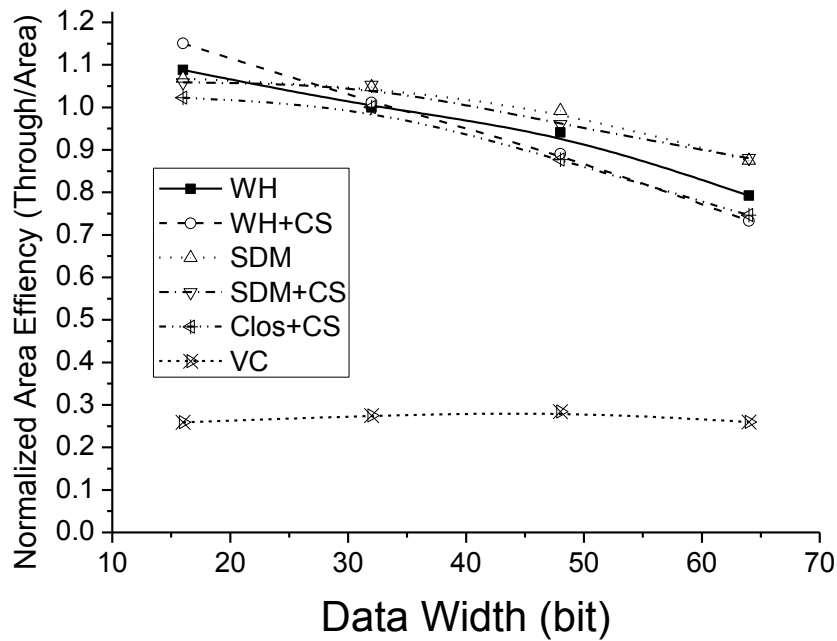
8x8 Mesh, XY routing algorithm, random uniform traffic



Different Data Widths



Different Data Widths



Conclusion

- Synchronization compromise throughput
 - Completion detection
 - Timing division multiplexing
- Spatial parallelism introduce no synchronization overhead
 - Channel slicing in the physical layer
 - Spatial division multiplexing in the switching layer
 - 2-stage Clos switch reduce the area overhead of SDM

Thanks for your attention.