MANCHESTER 1824
The University of Manchester

GAELS Project Meeting

Automatic Data Path Extraction

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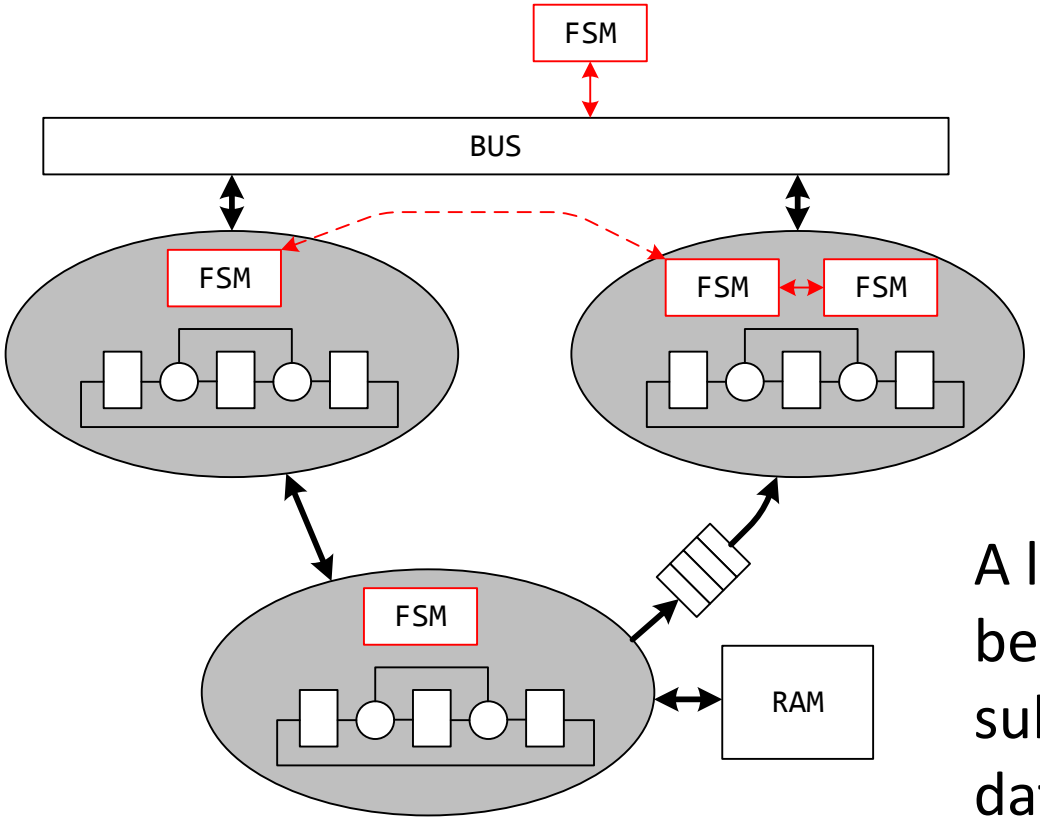
Content

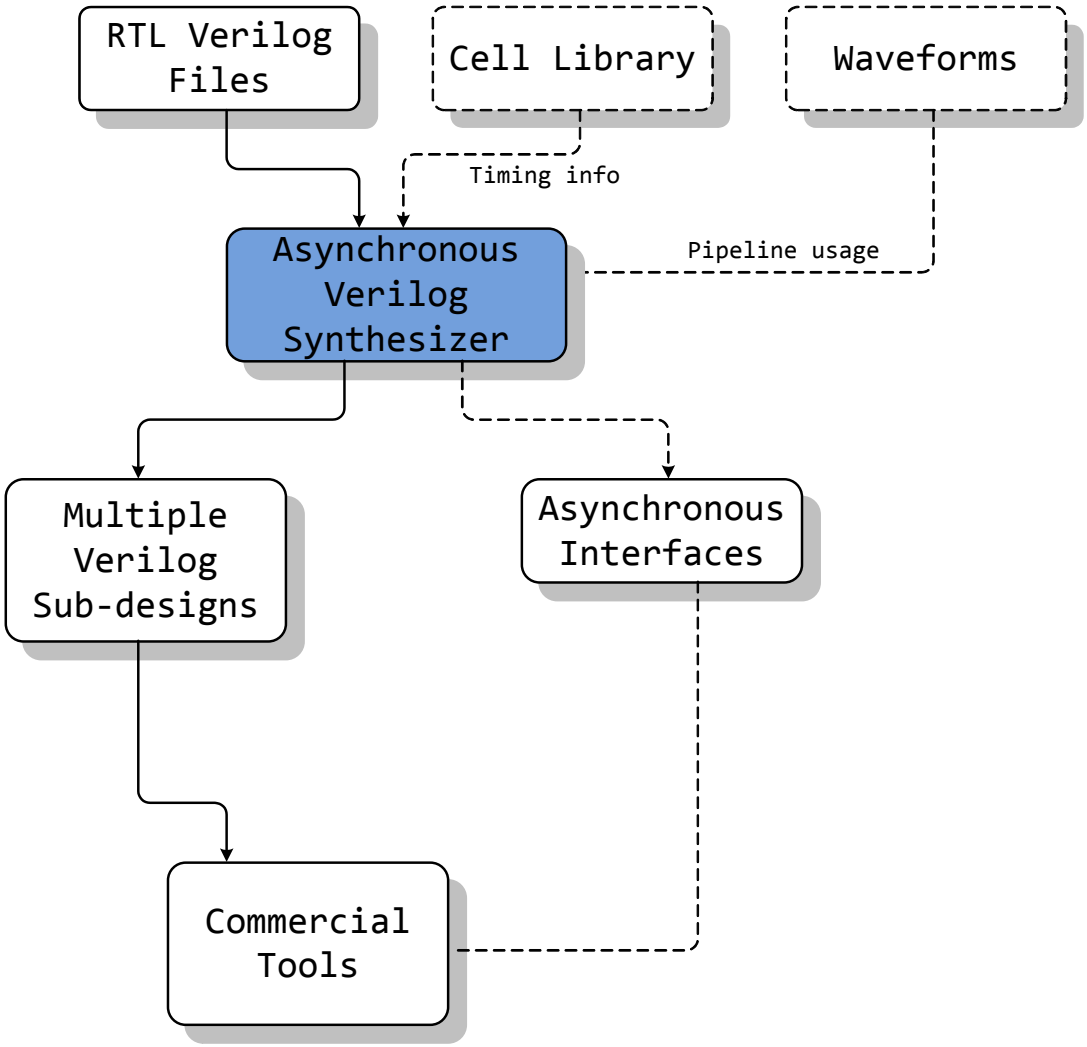
- Tool Flow
- Progress
  - Updated Type Calculation
  - Detailed FSM classification
  - Automatic Data Path Extraction
  - Preliminary Partition Analysis
- Future Works
- Conclusion

System Partitions

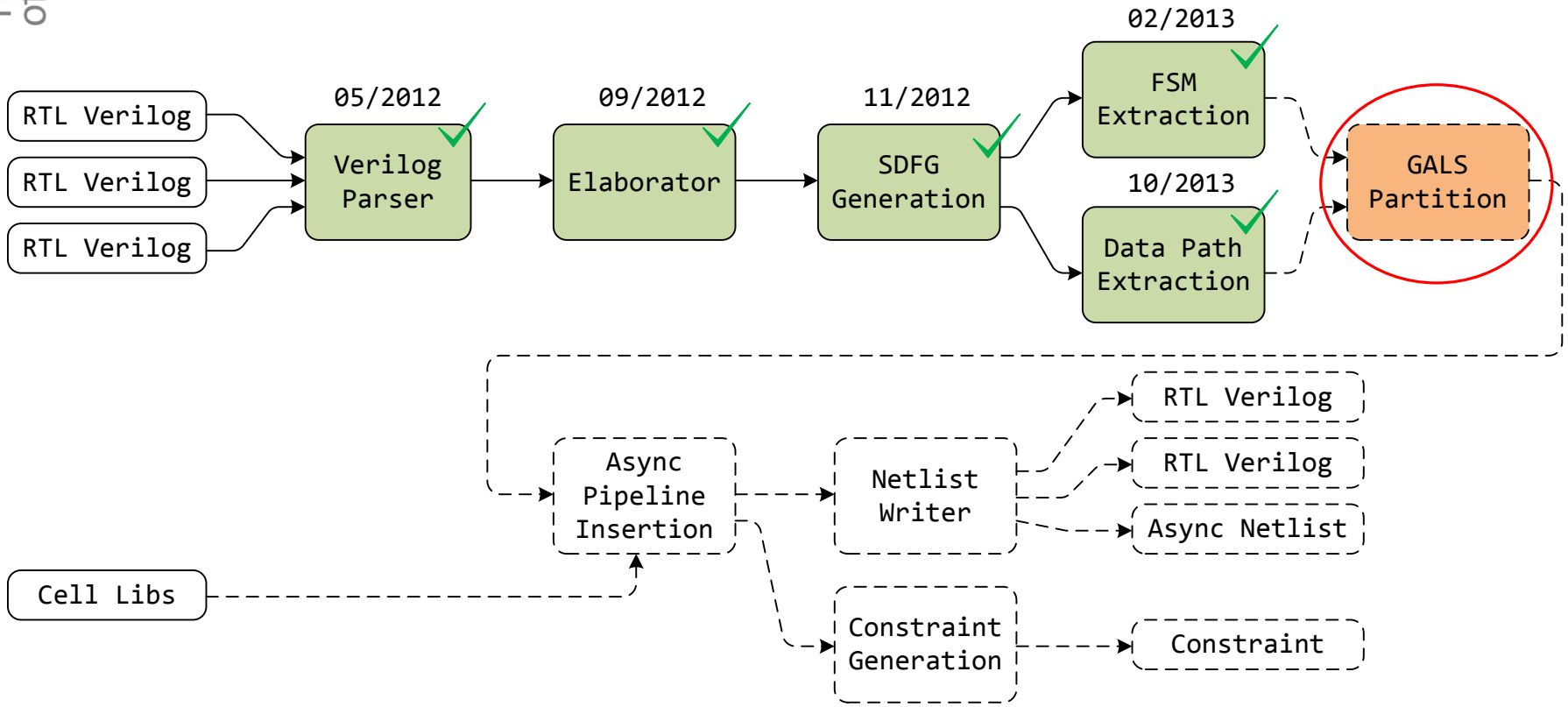


A large RTL system can be partitioned into multi sub-design connected by data channels with variable data-rates.

Tool Flow


RTL Verilog Files
Cell Library
Waveforms
Timing info
Asynchronous Verilog Synthesizer
Pipeline usage
Multiple Verilog Sub-designs
Asynchronous Interfaces
Commercial Tools

Flow inside Async Synthesizer

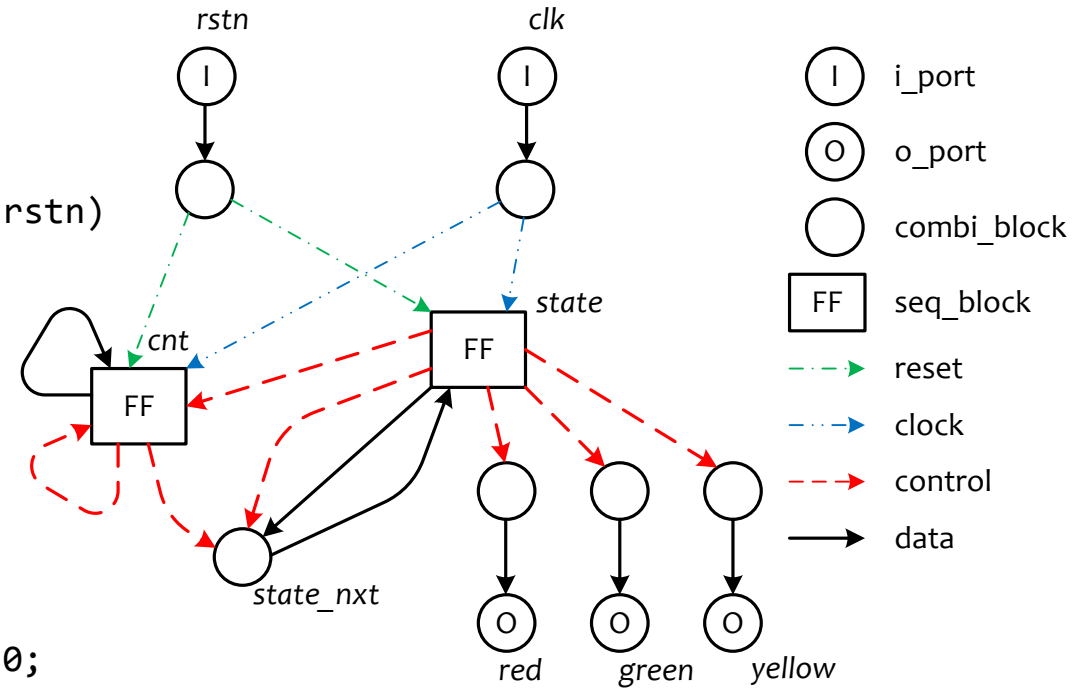


Progress from Last Meeting

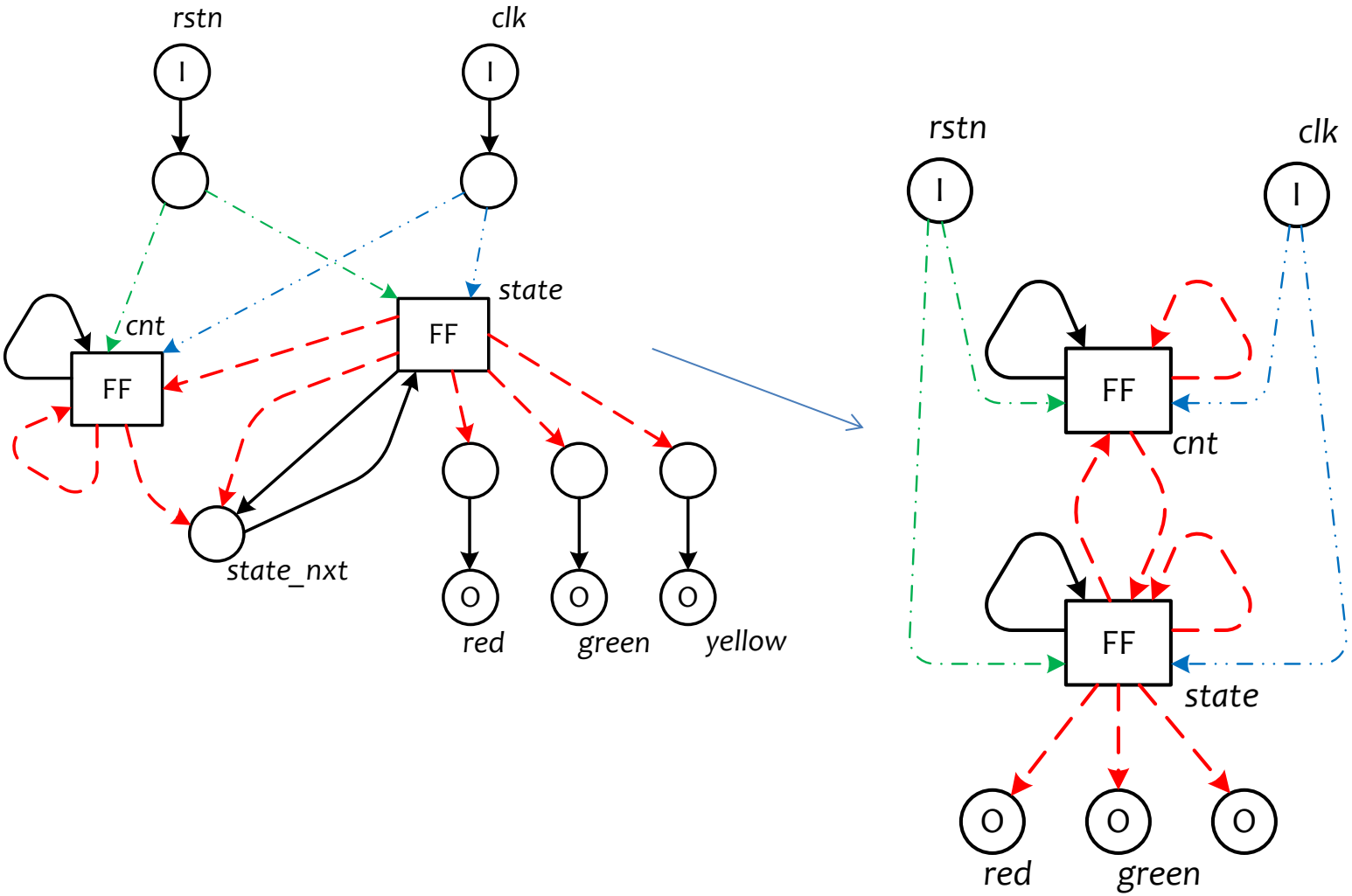
- Automatic FSM classification
  - Add more types in SDFG
  - Automatic identify FSMs, counters and flags.
- Automatic data path extraction
  - Removing control arcs
  - Trim the SDFG afterwards
- Preliminary partition analysis
  - All data outputs have variable data rate

Signal-Level Data Flow Graph

```
always @(posedge clk or negedge rstn)
  if(~rstn)
    state <= R;
  else
    state <= state_nxt;

always @(state or cnt) // next state
  if(cnt == 0)
    case(state)
    R:  state_nxt = YR;
    YR: state_nxt = G;
    G:  state_nxt = YG;
    default: state_nxt = R;
    endcase // case (state)
  else
    state_nxt = state;

always @(posedge clk or negedge rstn)
  if(~rstn)
    cnt <= 0;
  else if(cnt == 0)
    case(state)
    R:  cnt <= 2;
    YR: cnt <= 49;
    G:  cnt <= 4;
    default: cnt <= 49;
    endcase // case (state)
  else
    cnt <= cnt - 1;

assign red = state == R ? 1 : 0;
assign green = state == G ? 1 : 0;
assign yellow =
  (state == YR || state == YG) ? 1 : 0;
```



Register Relation Graph



Add Extra Arc Types

- Old typing systems
  - Data
  - Control
  - Clock; Reset
- New typing system
  - Self-loop; Calculation; Assign; Data*
  - Compare; Equate; Logic; Address; Control*
  - Clock; Reset

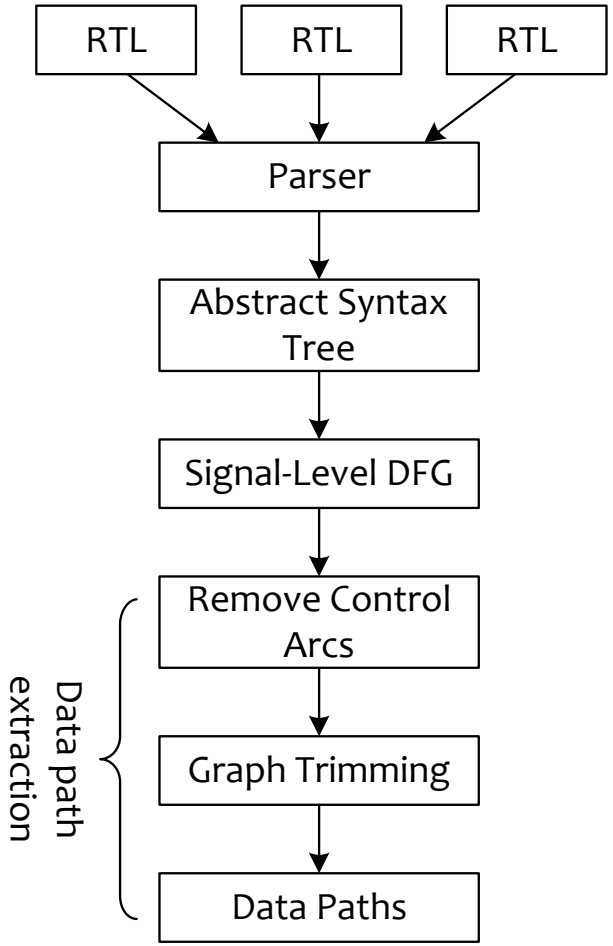
Recognition Criteria

- State machine
  - Self (equate); Out(equate); In(!data)
- Counter
  - Self(Calculate); Out(equate|compare|logic); In(!data)
- Address
  - Self(default); Out(address); In(!data)
- Flag
  - Self(All); Out(logic); In(!data)
- Other
  - Self(All); Out(control); in(!data)

FSM report

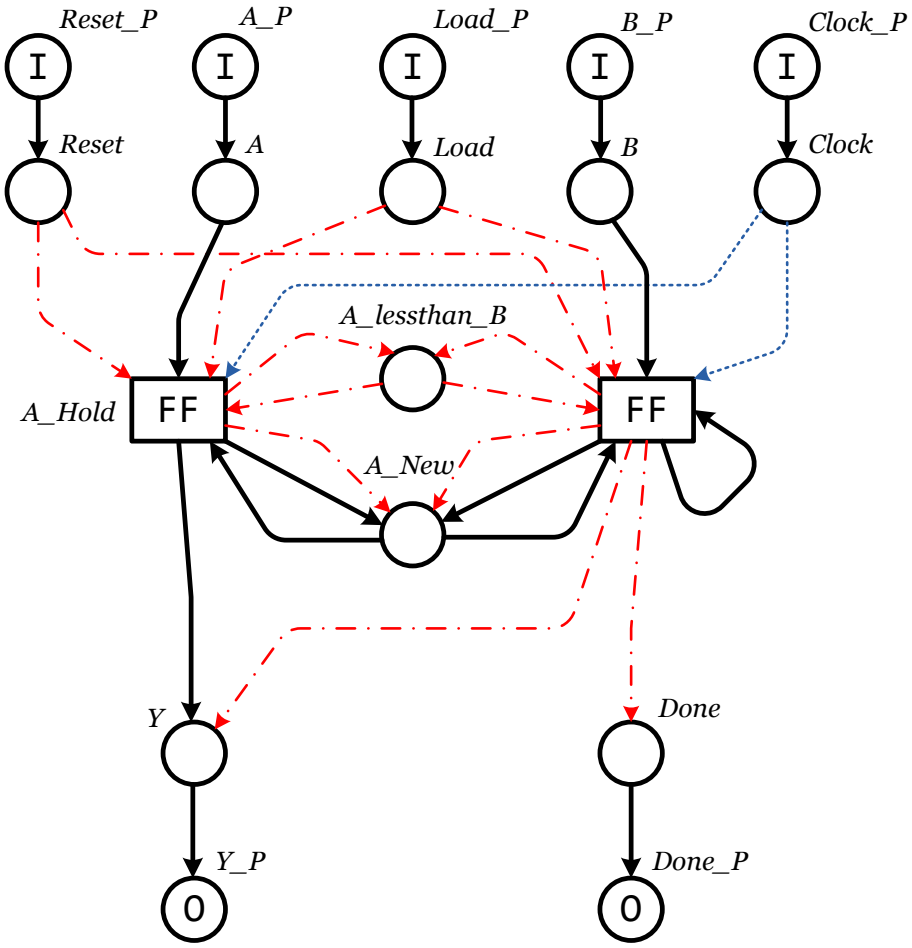
- SUMMARY:
- In this extraction, 2074 nodes has been scanned, in which 120 nodes are registers.
- **In total 30 FSM controllers has been found in 101 potential FSM registers.**
- The extracted FSMs are listed below:
- [1] dwb_biu/aborted_r FLAG
- [2] dwb_biu/valid_div CNT|FLAG
- [3] iwb_biu/aborted_r FLAG
- [4] iwb_biu/previous_complete FLAG
- [5] iwb_biu/valid_div CNT|FLAG
- [6] or1200_cpu/or1200_ctrl/sig_syscall FLAG
- [7] or1200_cpu/or1200_ctrl/sig_trap FLAG
- [8] or1200_cpu/or1200_except/delayed_iee FLAG
- [9] or1200_cpu/or1200_except/ex_dslot FLAG
- [10] or1200_cpu/or1200_except/except_type FSM|ADR
- **[11] or1200_cpu/or1200_except/extend_flush FSM|FLAG**
- [12] or1200_cpu/or1200_except/state FSM|FLAG
- [13] or1200_cpu/or1200_if/saved FLAG
- [14] or1200_cpu/or1200_mult_mac/div_free FLAG
- [15] or1200_cpu/or1200_operandmuxes/saved_a FLAG
- [16] or1200_cpu/or1200_operandmuxes/saved_b FLAG
- [17] or1200_dc_top/or1200_dc_fsm/cache_inhibit FLAG

Data Path Extraction

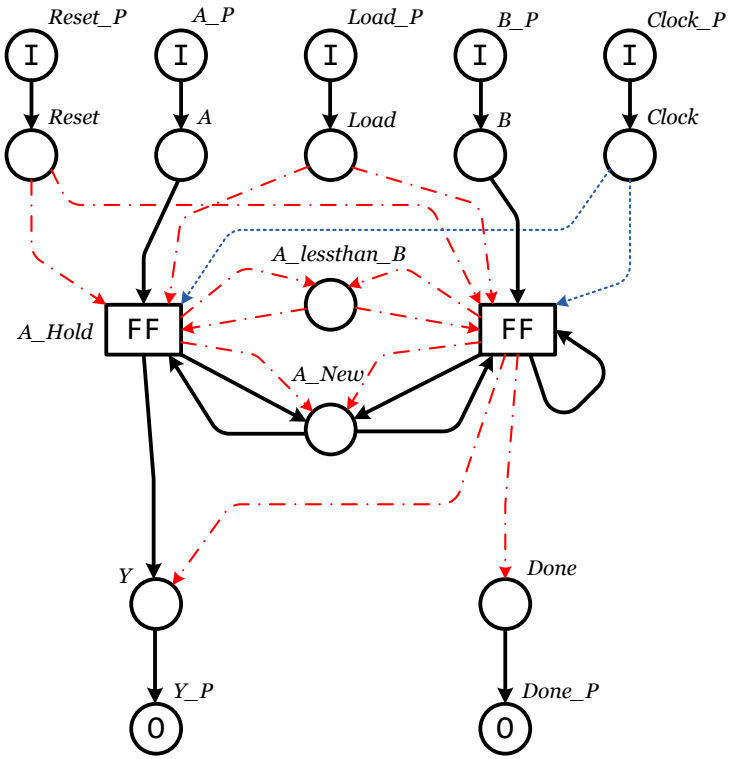


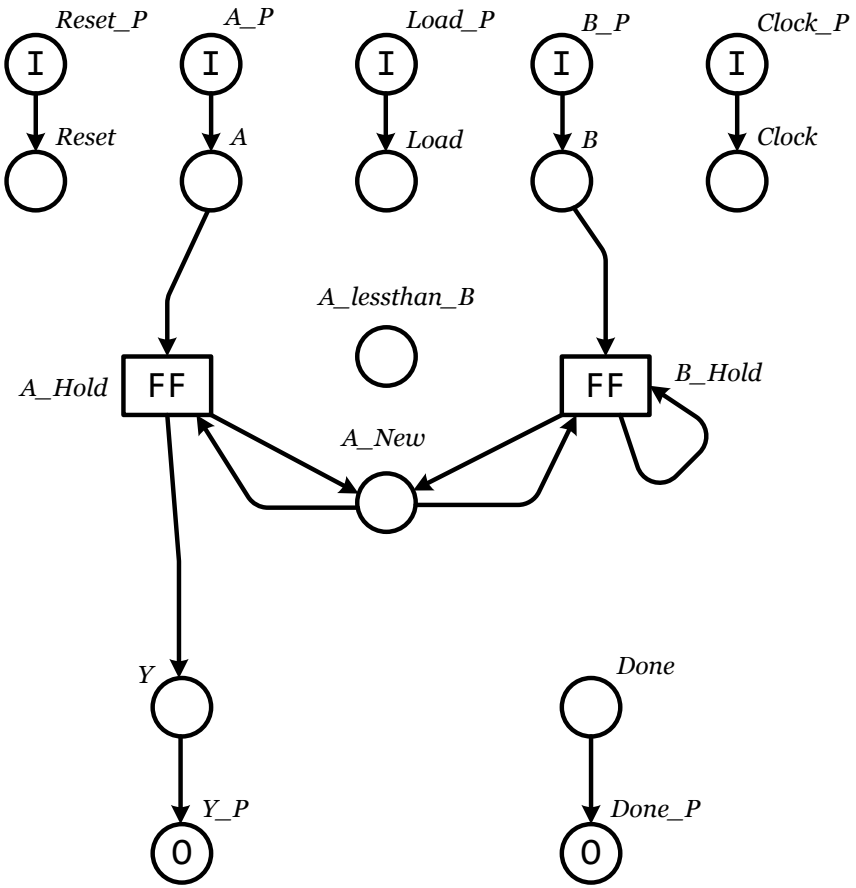
Greatest Common Divisor

```
module GCD (Clock,Reset,Load,A,B,Done,Y);
   input  Clock,Reset,Load;
   input  [7:0] A,B;
   output Done;
   output [7:0] Y;
   reg A_lessthan_B,Done;
   reg [7:0] A_New,A_Hold,B_Hold,Y;

   always @(posedge Clock)
     if(Reset) begin
        A_Hold = 0;
        B_Hold = 0;
     end else if(Load) begin
        A_Hold = A;
        B_Hold = B;
     end else if(A_lessthan_B) begin
        A_Hold = B_Hold;
        B_Hold = A_New;
     end else
        A_Hold = A_New;

   always @(A_Hold or B_Hold)
     if(A_Hold >= B_Hold) begin
        A_lessthan_B = 0;
        A_New = A_Hold - B_Hold;
     end else begin
        A_lessthan_B = 1;
        A_New = A_Hold;
     end

   always @(A_Hold or B_Hold)
     if(B_Hold == 0) begin
        Done = 1;
        Y = A_Hold;
     end else begin
        Done = 0; Y = 0;
     end
endmodule
```

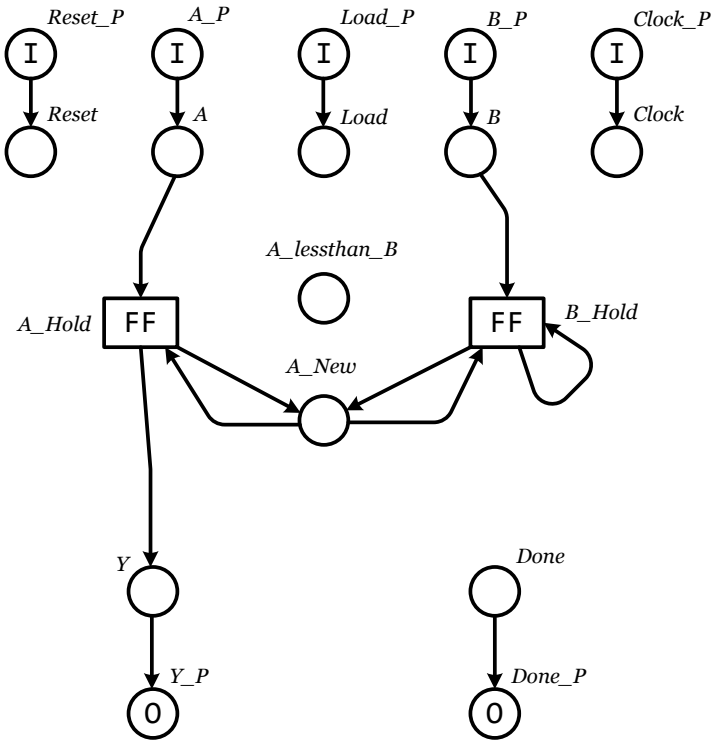


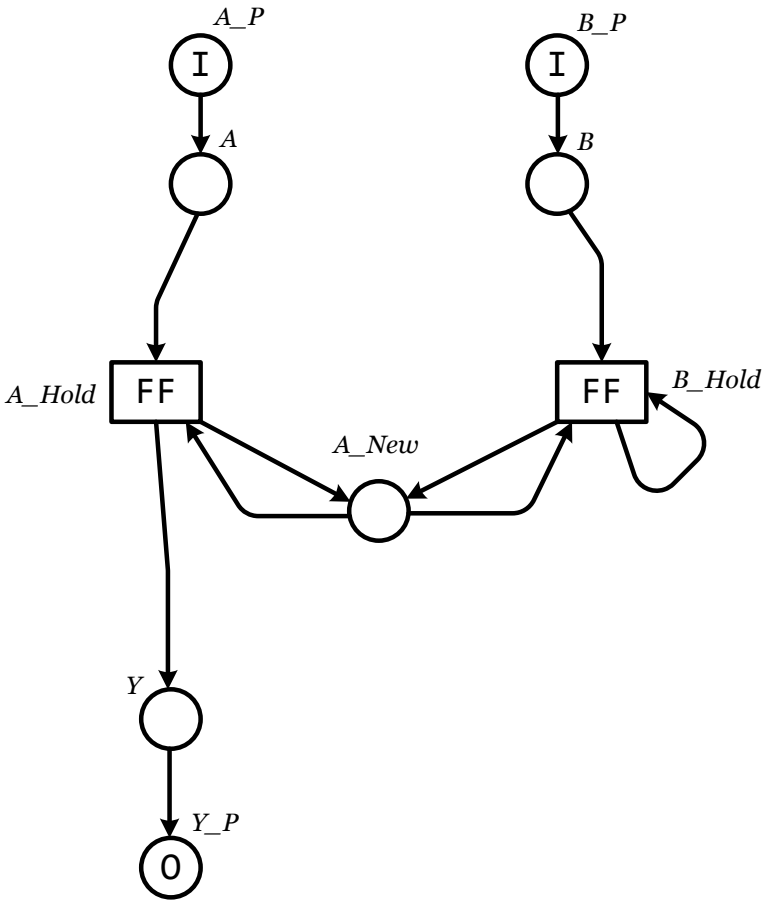
Remove Control Arcs



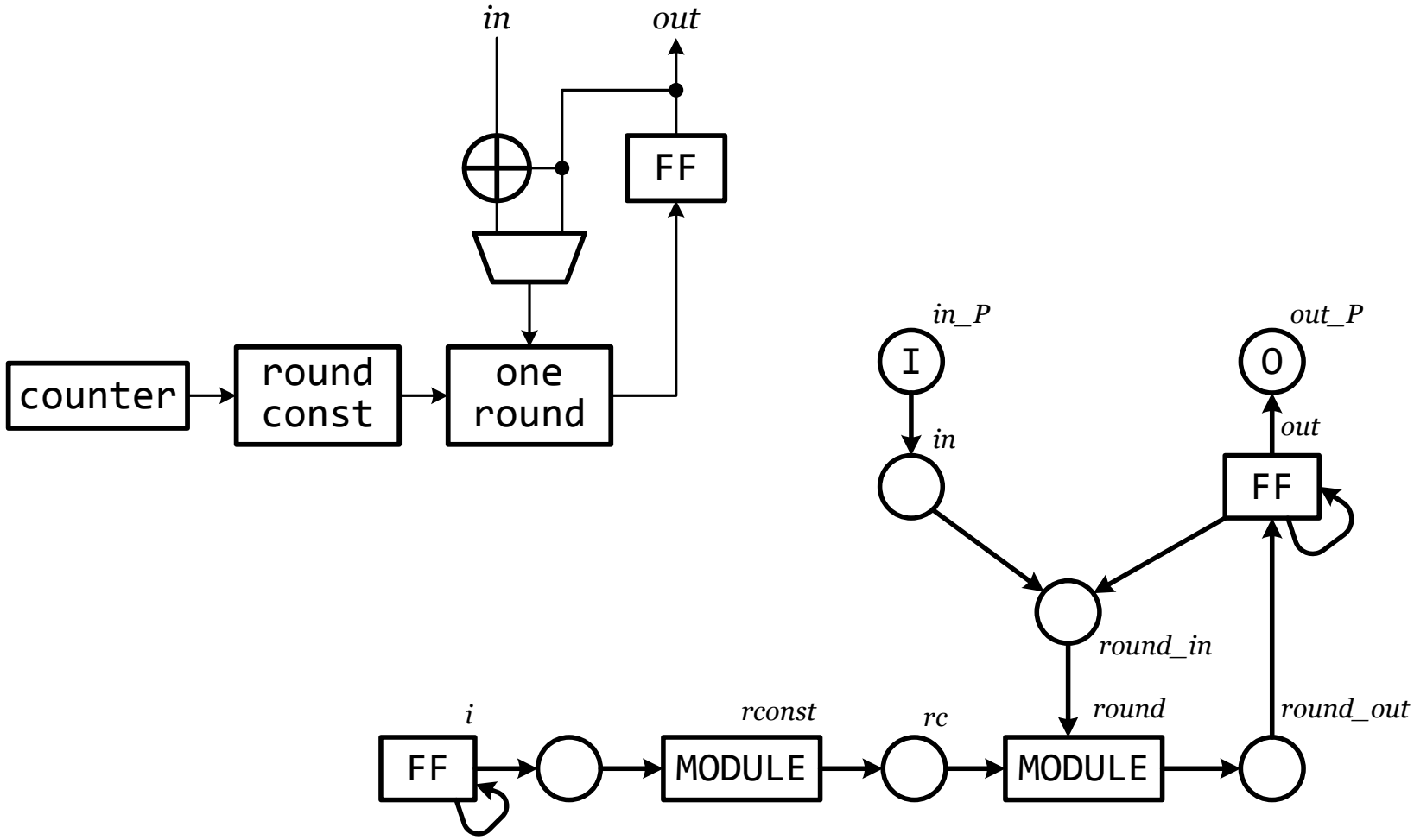


Trim the SDFG

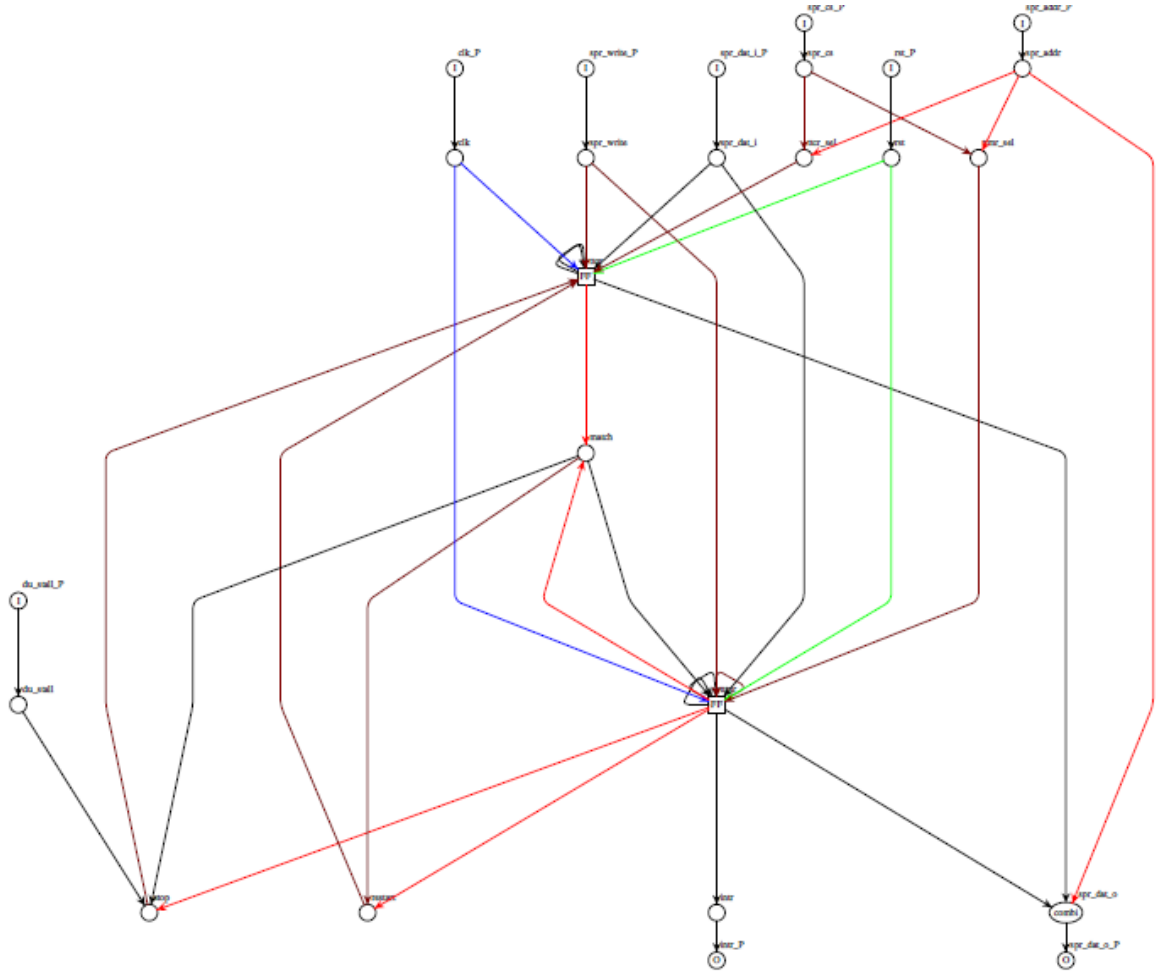


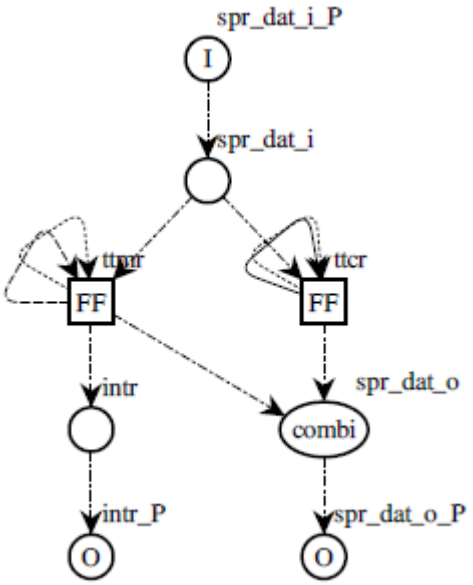


Permutation Module (SHA-3)



Large Scale Designs

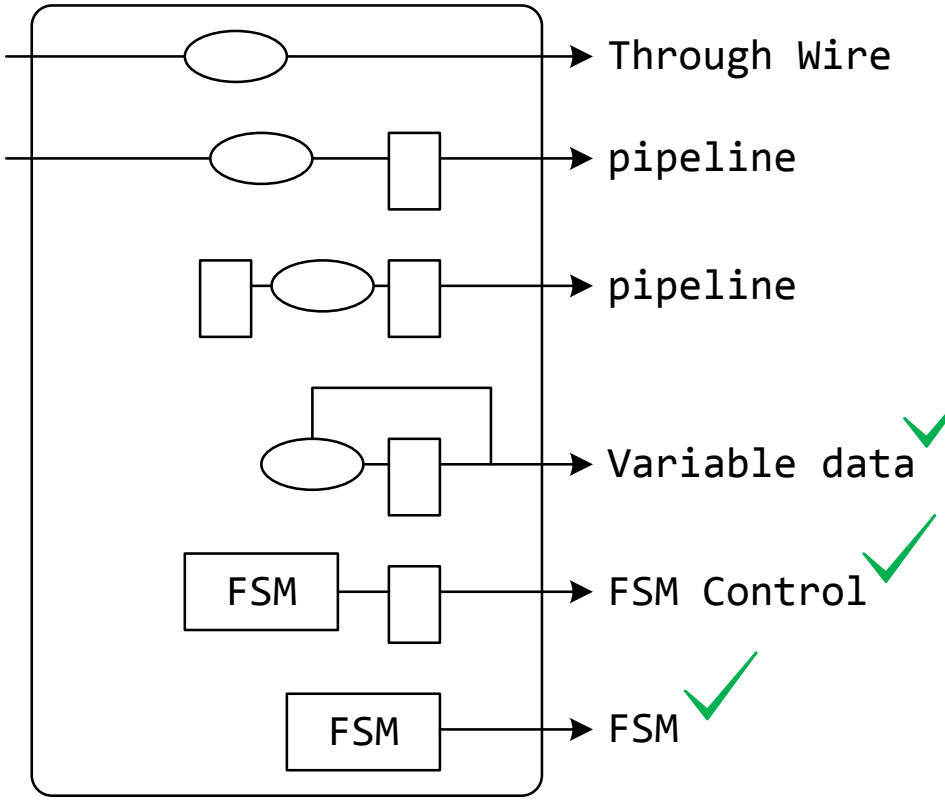




Performance

Design	Signal-level DFG			Extracted data path			Running
	I/O	Module	Signal	I/O	Module	Signal	time (s)
OR1200	52	37	2074	40	33	1142	1
RSD	7	24	1063	3	23	659	<1
NOVA	19	140	7043	9	103	4279	10

Partition Detection



Classify each output port as fixed rate (through wire or pipeline) or variable rate (variable data, FSM control, FSM)

A Module with most output ports with variable rate is considered a potential partition.

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Partition Detection Report

```
pixel_generator  (module vga_pgen) with rate 0.470588 < 0.8:
    hsync_o                 0       [pixel_generator/hsync_o:data-pipeline]
    cc0_adr_o               0       [through wire]
    cc1_adr_o               0       [through wire]
    stat_acmp               1       [pixel_generator/stat_acmp:self-fsm:ctl-
fsm(pixel_generator/stat_acmp)]
    blank_o                 0       [pixel_generator/blank_o:data-pipeline]


wbm/clut_sw_fifo (module vga_fifo_aw4_dw1) with rate 1 >= 0.8:
    aempty                  1       [wbm_ack_i_P:data-
pipeline][pixel_generator/color_proc/vdat_buffer_rreq:ctl-
fsm(pixel_generator/rgb_fifo/nword]
    full                    1       [wbm/clut_sw_fifo/full:ctl-
fsm(wbm/stb_o,wbm/clut_sw_fifo/rp,wbm/clut_sw_fifo/wp)]
    empty                   1       [wbm/clut_sw_fifo/empty:ctl-
fsm(wbm/stb_o,wbm/clut_sw_fifo/rp,wbm/clut_sw_fifo/wp)]
    nword                   1       [wbm/clut_sw_fifo/nword:ctl-fsm(wbm/stb_o)]
    afull                   1       [wbm_ack_i_P:data-
pipeline][pixel_generator/color_proc/vdat_buffer_rreq:ctl-
fsm(pixel_generator/rgb_fifo/nword,pixel_generator/color_proc/colcnt]
```

Future Works

- Partition Detection
  - Rather than evaluate all output ports, evaluate only data output ports.
  - Replace the pattern detection with data rate estimation (possibly need state space analyses)
  - Back-annotate data rate to data path graph
  - Interface recognition (mem, FIFO, handshake, bus, etc)

Conclusion

- Utilizing signal-level data flow graph, the sync Verilog synthesizer is able to:
  - Detect and classify controllers
  - Detect data paths
  - Detect potential partitions (preliminary)