Wei Song, PhD, Associate Professor

CONTACT INFORMATION

Institute of Information Engineering
Chinese Academy of Sciences
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ACADEMIC EXPERIENCE

Institute of Information Engineering, CAS, Beijing, P.R.China

November 2017 to present
Associate Processor

- Enhance system security with new processor and cache micro-architectures. **(11/2017 — present)**
  - Defense control flow hijacking with hardware managed tagged memory.
  - Avoid cache side-channel attacks with new cache architectures.
  - Evluating the vulnerabilities of a hardware system using a systemic test suite.

University of Cambridge, Cambridge, UK

November 2014 to October 2017
Research Associate, Computer Laboratory

- LowRISC: An open-source SoC hardware platform using the 64-bit RISC-V ISA. **(11/2014 — 10/2017)**
  - Added tagged memory support to Rocket SoC (L1 D$, L2 and tag cache).
  - Added memory mapped IO support to Rocket core.
  - Untethered Rocket chip SoC.
  - Booted a RISC-V Linux on the untethered Rocket chip using KC705 and Nexys4-DDR boards.
- Large-scale sorter on FPGA for database applications. **(9/2013 — 10/2016)**
  - Parallel merge-sorters to break the speed limit of sequential sorters [25].

The University of Manchester, Manchester, UK

October 2011 to October 2014
Research Associate, School of Computer Science

- EPSRC Project EP/L000563/1: Continuous on-line adaptation in many-core systems: From graceful degradation to graceful amelioration. **(9/2014 — 10/2014)**
  - Investigate the intra/inter-chip task (neuron) migration in the SpiNNaker many-core system.
- EPSRC Project EP/I038306/1: Globally Asynchronous Elastic Logic Synthesis. **(10/2011 — 9/2014)**
  - Implemented a RTL Verilog HDL parser using Bison and Flex.
  - Automatic finite state machine (FSM) detection using register relation graphs [18].
  - Automatic data-path extraction using signal-level data flow graphs [19].
  - Automatic interface type recognition.
  - cppRange: A multi-dimensional range calculation library.
- Fault-tolerance techniques for asynchronous on-chip networks. **(9/2012 — 9/2014)**
  - Redundent code for QDI 1-of-N pipeline to avoid errors caused by 1-bit transient fault [17,23].
  - Detect and recover from the deadlock caused by permanent faults in asynchronous SDM routers [20,21,24,26].

September 2007 to September 2011
Ph.D. in Computer Science, School of Computer Science

- Supervisor: Dr. Doug Edwards

- EPSRC Doctoral Training Award EP/P503833/1 (10/2007–3/2011)
  EPSRC Project Grant EP/E06065X/1 (4/2008–7/2011)
  Bursary of the School of Computer Science, Univ. of Manchester (10/2007–3/2011)
- Thesis: *Spatial parallelism in the routers of asynchronous on-chip networks*
  - Designed and implemented asynchronous spatial division multiplexing (SDM) routers for asynchronous on-chip networks [13,15].
  - Designed and implemented a high-speed asynchronous wormhole router for asynchronous on-chip networks [9,11].
  - Designed and implemented the first asynchronous scheduler for three-stage S^3 Clos networks [12,14].
  - All designs are coded in synthesizable Verilog HDL (Faraday 130nm cell library), implemented by Synopsys DC-Topo, ICC, StarXRC, PrimeTime-PX, and simulated by SystemC/Verilog co-simulation using Cadence NC-Sim.

Beijing University of Technology, Beijing, P.R.China

September 2005 to September 2008
M.S.EE. in Automation, College of Electronic Information and Control Engineering

- Designed and implemented an ANSI C non-preemptive real-time scheduler [2,3,7,10] for the central controller of electrical vehicles. (supported by Beijing Sci. Foundation #KZ20041000501).

October 2004 to November 2006
Research Assistant, Beijing Embedded System Key Lab

- Implementing the ASIC prototypes into FPGA verification platforms for the final hardware test before tape out. FPGA platforms include Xilinx Virtex-4 and II. ASIC prototypes include the baseband for ATSC, DVB-T, DVB-C and WLAN 802.11g.

September 2001 to September 2005
B.S.EE. in Automation, College of Electronic Information and Control Engineering
Minor in Computer Science, College of Computer Science

PUBLICATIONS

2017

26 Guangda Zhang, **Wei Song**, Jim Garside, Javier Navaridas, and Zhiying Wang. **Handling physical-layer deadlock caused by permanent faults in quasi-delay-insensitive network-on-chip**. IEEE Transactions on Very Large Scale Integration Systems (TVLSI), Vol. 25, No. 11, pp. 3152-3165, November 2017.

2016

25 **Wei Song**, Dirk Koch, Mikel Luján, and Jim Garside. **Parallel hardware merge sorter**. In *Proc. of International Symposium on Field-Programmable Custom Computing Machines (FCCM)*, Washington DC, United States, pp. 95–102, May 2016.

2015

24 Guangda Zhang, Jim Garside, **Wei Song**, Javier Navaridas, and Zhiying Wang. **Deadlock recovery in asynchronous networks on chip in the presence of transient faults**. In *Proc. of International Symposium on Asynchronous Circuits and Systems (ASYNC)*, CA, United States, pp. 100–107, May 2015.

2014

23 Guangda Zhang, **Wei Song**, Jim Garside, Javier Navaridas, and Zhiying Wang. **Protecting QDI interconnects from transient faults using delay-insensitive redundant check codes**. *Microprocessors and Microsystems*, Vol. 38, No. 8, pp. 826–842, November 2014.

22 Oriol Arcas Abella, Geoffrey Ndu, Nehir Sonmez,Mohsen Ghasempour,Adria Armejach, Javier Navaridas, **Wei Song**, John Mawer, Adrian Cristal, and Mikel Lujan. **An empirical evaluation of high-level synthesis languages and tools for database acceleration**. In *Proc. of International Conference on Field Programmable Logic and Applications (FPL)*, Munich, Germany, pps. 8, September 2014.

21 Guangda Zhang, **Wei Song**, Jim Garside, Javier Navaridas, and Zhiying Wang. **An asynchronous SDM network-on-chip tolerating permanent faults**. In *Proc. of International Symposium on Asynchronous Circuits and Systems (ASYNC)*, Potsdam, Germany, pp. 9–16, May 2014.

20 **Wei Song**, Guangda Zhang, and Jim Garside. **On-line detection of the deadlocks caused by permanently faulty links in quasi-delay insensitive networks on chip**. In *Proc. of International Conference of the Great Lakes Symposium on VLSI (GLSVLSI)*, Houston, Texas, USA, pp. 211–216, May 2014.

19 **Wei Song**, Jim Garside, and Doug Edwards. **Automatic data path extraction in large-scale register-transfer level designs**. In *Proc. of IEEE International Symposium on Circuits and Systems (ISCAS)*, Melbourne, Australia, pp. 377–380, June 2014.

2013

18 **Wei Song** and Jim Garside. **Automatic controller detection for large scale RTL designs**. In *Proc. of EUROMICRO Conference on Digital System Design (DSD)*, Santander, Spain, pp. 884–851, September 2013.

17 Guangda Zhang, **Wei Song**, Jim Garside, Javier Navaridas, and Zhiying Wang. **Transient fault tolerant QDI interconnects using redundant check code**. In *Proc. of EUROMICRO Conference on Digital System Design (DSD)*, Santander, Spain, pp. 3–10, September 2013.

2012

16 **Wei Song** and Doug Edwards. **Survey of asynchronous networks-on-chip**. *Journal of Computer-Aided Design & Computer Graphics*, Vol. 24, No. 6, pp. 699–709, 2012. (Chinese)

15 **Wei Song**, Doug Edwards, Jim Garside, and William J. Bainbridge. **Area efficient asynchronous SDM routers using 2-stage Clos switches**. In *Proc. of Design, Automation & Test in Europe (DATE)*, Dresden, Germany, pp. 1495–1500, March 2012.

2011

14 **Wei Song**, Doug Edwards, Zhenyu Liu, and Sohini Dasgupta. **Routing of asynchronous Clos networks**. *IET Computers & Digital Techniques*, Vol. 5, No. 6, pp. 452–467, 2011.

13 **Wei Song** and Doug Edwards. **Asynchronous spatial division multiplexing router**. *Microprocessors and Microsystems*, Vol. 35, No. 2, pp. 85–97, 2011.

Earlier

12 **Wei Song** and Doug Edwards. **An asynchronous routing algorithm for Clos networks**. In *Proc. of International Conference on Application of Concurrency to System Design (ACSD)*, Braga, Portugal, pp. 67–76, June 2010.

11 **Wei Song** and Doug Edwards. **A low latency wormhole router for asynchronous on-chip networks**. In *Proc. of Asia and South Pacific Design Automation Conference (ASP-DAC)*, Taipei, TAIWAN, pp. 437–443, January 2010.

10 Zhe Xu, Shizhen Yan, **Wei Song**, Chunxuan Yu, Jianmin Duan, and Mingjie Zhang. ***A method to implement the CANopen master***. Chinese invention patent, Application No. CN200810056824.5, Grant No. CN101222510B, November 2010.

9 **Wei Song** and Doug Edwards. **Building asynchronous routers with independent subchannels**. In *Proc. of International Symposium on SoC*, Tampere, Finland, pp. 48–51, October 2009.

8 **Wei Song**, Doug Edwards, Jose Luis Nunez-Yanez, and Sohini Dasgupta. **Adaptive stochastic routing in fault-tolerant on-chip networks**. In *Proc. of ACM/IEEE International Symposium on Networks-on-Chip (NoCS)*, San Diego, CA, USA, pp. 32–37, May 2009.

7 Zhe Xu, Shizhen Yan, **Wei Song**, and Zhuo Zhang. **Development of the CANopen master based on MC9S12DP512 and μC/OS-II**. *Computer Engineering and Science*, Vol. 31, No. 5, pp. 118–120, 2009. (Chinese)

6 Zhe Xu, Shizhen Yan, and **Wei Song**. **Object dictionary design of CANopen based on hash table**. *Computer Engineering*, Vol. 35, No. 8, pp. 44–46, 2009 (Chinese).

5 **Wei Song**, Suiming Fang, Dan Yao, Lichao Zhang, and Cheng Qian. Clock synchronization in multi-FPGA designs. *Computer Engineering*, Vol. 34, No. 7, pp. 245–247, 2008 (Chinese).

4 **Wei Song**, Suiming Fang, Mingjie Zhang, and Zhe Xu. **Task scheduler in the design of CANopen master**. *Computer Measurement & Control*, Vol. 16, No. 4, pp. 558–560, 2008 (Chinese).

3 **Wei Song**, Shizhen Yan, Zhe Xu, and Suiming Fang. **Transplantable CANopen master based on non-preemptive task scheduler**. In *Proc. of IEEE International Conference on Automation and Logistics (ICAL)*, Jinan, P.R.China, pp. 557–562, August 2007.

2 **Wei Song** and Suiming Fang. Clock circuit design in FPGA based on BUFGMUX and DCM. *Modern Electronic Technique*, Vol. 29, No. 2, pp. 141–143, 2006. (Chinese)

1 **Wei Song**. **The method of using m-files of MATLAB6.5 in C language**. *Computer and Information Technology*, Vol. 7, No. 12, pp. 57–58, 2004. (Chinese)

Open-source Projects

lowRISC, member, ongoing
Providing an open-source SoC platform using the 64-bit RISC-V ISA.
https://github.com/lowRISC

Open SoC Debug, contributor, ongoing
Providing building blocks for SoC debug systems.
https://github.com/opensocdebug

Asynchronous Verilog Synthesiser, beta, developing stopped
Generate elastic or asynchronous circuits from synchronous RTL designs written in Verilog HDL.
https://github.com/wsong83/Asynchronous-Verilog-Synthesiser

cppSaif, stable
A C++ library for parsing SAIF (Switching Activity Interchange Format) files.
https://github.com/wsong83/cppSaif

C++/Tcl, stable
A C++ library for interoperability between C++ and Tcl.
Adopted from the original C++/Tcl designed by Maciej Sobczak.
https://github.com/wsong83/cpptcl

VPreproc, stable
A standalone C++ preprocessor for the Verilog HDL language.
Adopted from the Verilog Perl tool suite designed by Wilson Snyder.
https://github.com/wsong83/vpreproc

Asynchronous Spatial Division Multiplexing (SDM) Router, stable
Hardware designs of asynchronous SDM routers using Nangate 45nm cell library. Gate-level, synthesisable netlist written in Verilog HDL. SystemC testbenches and synthesis scripts for Synopsys DC provided.
http://opencores.org/project,async_sdm_noc

Academic Activities

IEEE Member

Reviewer for:
EURASIP Journal on Embedded Systems
IEEE Communications Letters
IEEE Transactions on Parallel and Distributed Systems
IET Computer and Digital Techniques
Journal of Computers
Journal of Parallel and Distributed Computing
Microprocessors and Microsystems

Teaching Experience

Computer Laboratory, the University of Cambridge, Cambridge, UK

Lab Demonstrator

- *ECAD and Architecture Practical Classes*, Part IB (2nd year undergraduate), 2016

Supervisor (small group tutor)

- *Comparative Architectures*, Part II (3rd year undergraduate), 2016, 2017

- *System-on-Chip Design*, Part II (3rd year undergraduate), 2016, 2017

School of Computer Science, the University of Manchester, Manchester, UK

Graduate Student Lab Demonstrator

- *Microcontrollers*, 2nd year undergraduate, 2008, 2013
- *Fundamentals of Computer Engineering*, 1st year undergraduate, 2010
- *VLSI System Design*, 2nd year undergraduate, 2007, 2008, 2009, 2010
- *Fundamentals of Computer Architecture*, 1st year undergraduate, 2008, 2009, 2010
- *Mobile Systems*, 2nd year undergraduate, 2010
- *Operating Systems*, 2nd year undergraduate, 2009

TECHNICAL SKILLS

Hardware implementation flow
- TLM/RTL/Gate hardware design
- UVM/SystemVerilog/VHDL/SystemC/C++ mixed simulation
- ASIC and FPGA: synthesis, place and routing

Languages
- Verilog/VHDL, C/C++, SystemC, System Verilog, Chisel, MATLAB

Tools
- Cadence: NC-Sim, SoC encounter, Virtuoso
- Synopsys: Design Compiler, IC Compiler, VCS, Hspice, Nanosim
- Mentor: QuestaSim/ModelSim
- FPGA: Xilinx Vivado/ISE, Synpicity Synplify, Altera Quartus II