System-on-Chip Design Supervision Problem (Set 2)

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You can draw diagrams if feel necessary but using Verilog is preferred. Please keep your answers organised and tidy. If you could not answer some questions or would like a discussion during the supervision session, please label it in your answer.

SP 4. RTL, simulation, and hazards

Q1: Convert the following behavioural RTL into an equivalent one using only non-blocking assignments.

```
always @(posedge clk) begin
   foo = bar + 22;
   if (foo > 17)
      foo = 17;
   foo_final = foo;
   foo = 0;
end
```

Q2: Give a fragment of RTL that implements a counter that wraps after 7 clock ticks.

Q3: Implement a 16-bit multiplier that uses only 8-bit multipliers and adders. The finished multiplier should be fully pipelined, producing a result in every cycle with a 2 cycles delay and using the minimal number of 8-bit multipliers. (You can use * and + to represent an 8-bit multiplier and an adder respectively)

Q4: [optional] Implement a FIFO with a depth of 8. The width of data is 16-bit, and the FIFO has full and empty signals.

SP 5. Assertion based design

Q5: What is the difference between a safety and liveness assertion over the behavior of system? How can safety and liveness assertions be used in dynamic validation? Give a short segment of RTL that contains an imperative assertion that holds and give also a pair of valid safety and liveness assertions that holds.

Q6: What is the difference between black box testing and white box testing? Can assertions be used for black box testing?

Q7: What is “assertion based design”? What is the meaning of coverage? Explain how certain assertions can be reused at different layers of modeling abstraction.

Q8: What is a combinational equivalence problem and what is a sequential equivalence problem? Why might sequential equivalence be violated? And why might we see false negatives in a sequential equivalence checker?