Comparative Architectures Supervision Problem (Set 4)

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The following problems are mostly open-ended. Diagrams or charts are not needed in the answers. Therefore it is highly recommended to type the answers. Please keep your answers organised and tidy. If you feel difficult to answer some questions or would like a discussion during the supervision session, please label it in your answer.

Lecture 12 & 13. Chip multiprocessor

Q1. Why is a shared second-level (L2) cache typically divided into multiple banks (banked) in a chip multiprocessor?

Q2. In what situation might a shared second-level cache offer a performance advantage over a memory hierarchy for a chip multiprocessor with private L2 caches?

Q3. A cache controller in a chip multiprocessor snoops the bus and observes a transaction that refers to a block that its cache contains. The block is held in State M (Modified). The bus transaction has been generated by a processor wishing to read the block. Assuming a MSI (write-back invalidate) cache coherence protocol, what actions will be taken by the cache controller?

Q4. How does adopting an inclusion policy simplify the implementation of a cache coherence mechanism in a chip multiprocessor with private L1 and L2 caches?

Q5. How might multiple buses be exploited to enable a greater number of processors to be supported by a snoopy cache coherence protocol?

Q6. Why might we use a directory-based cache coherency protocol in preference to a snoopy protocol?

Q7. What optimisation does the addition of the E state to the MSI protocol provide?

Lecture14. On-chip interconnect

Q8. For what reasons might virtual-channels be added to an on-chip network?

Q9. Why might an adaptive routing algorithm offer better performance than a deterministic one?

Q10. How might the choice of cache coherence protocol influence the design of the on-chip network?

Lecture15. Special-purpose architectures

Q11. How can performance be improved while reducing power consumption?