

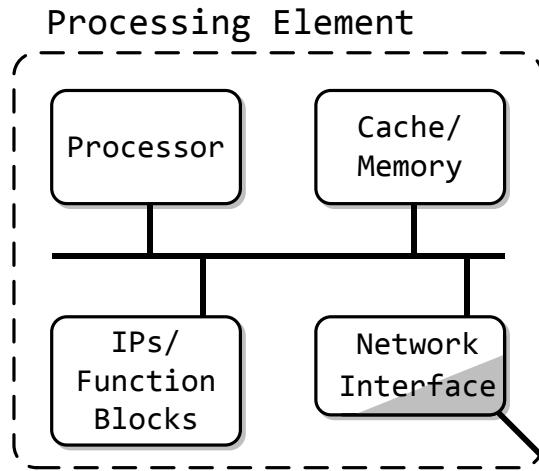
Using Clos Switches in Area Efficient Asynchronous SDM Routers

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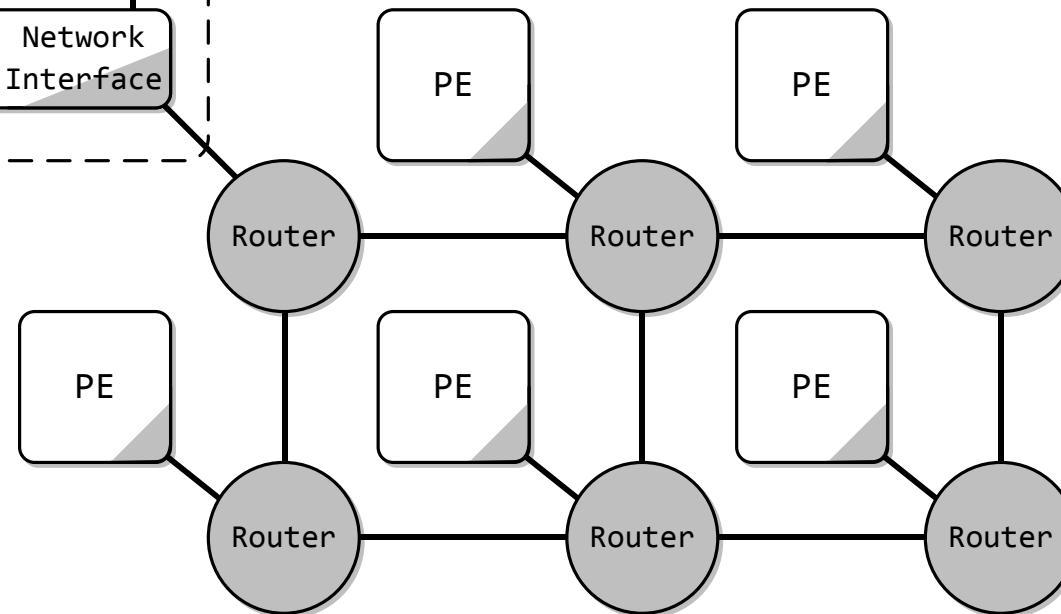
- Asynchronous Network-on-Chip
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Asynchronous Network-on-Chip

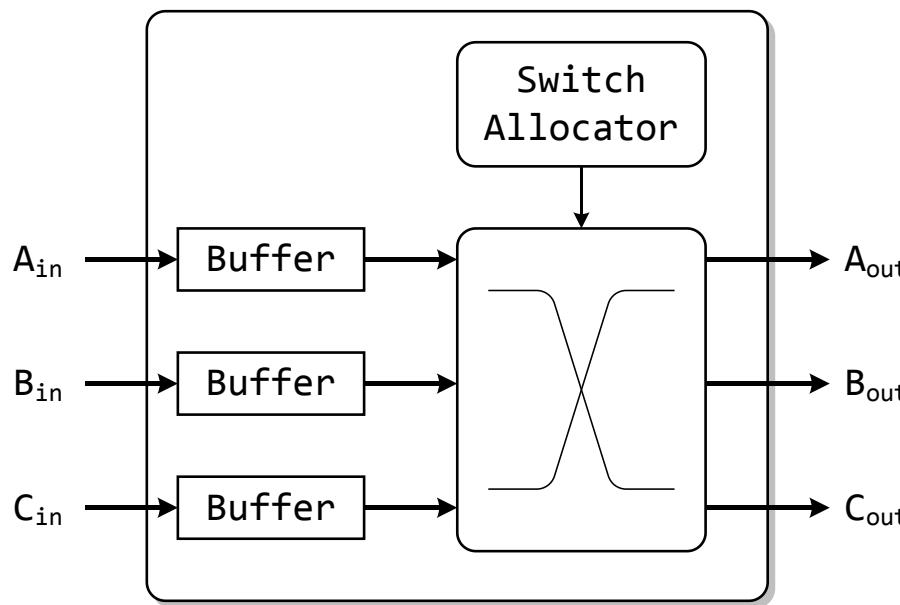


Network-on-Chip (NoC) or *on-chip network* is the state-of-the-art on-chip communication structure for multiprocessor systems.

GALS:
Globally
asynchronous
and locally
synchronous



Basic Router Structure

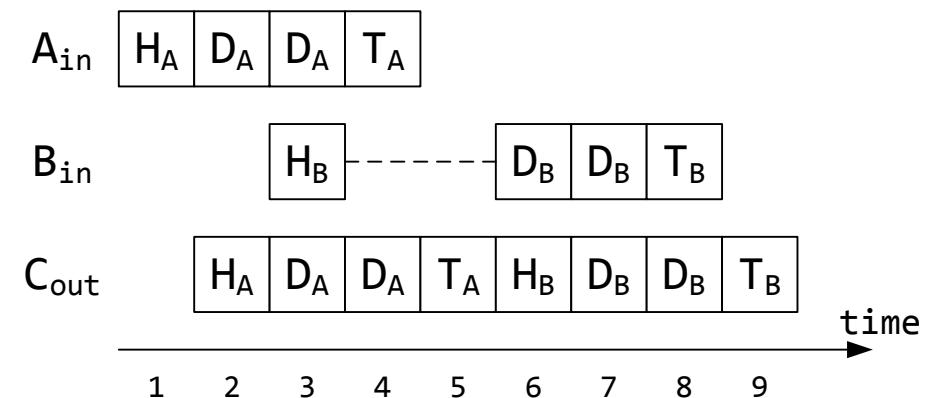


Flow control:

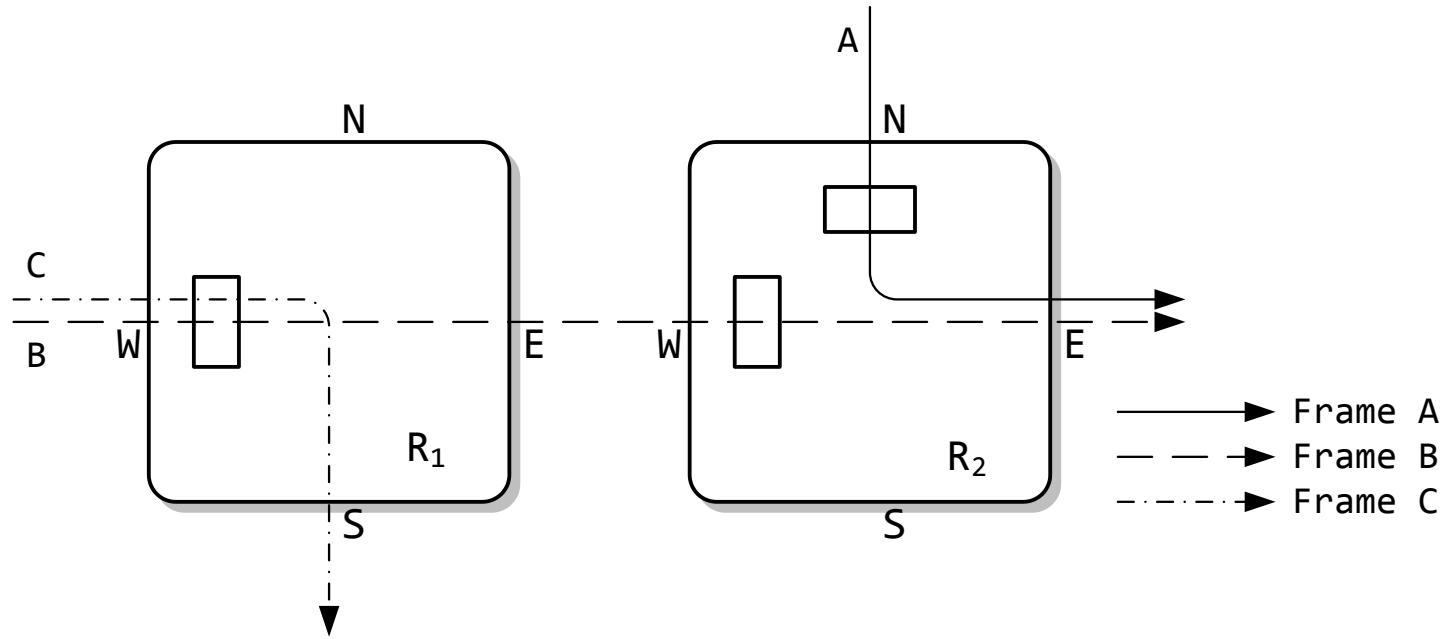
The algorithm used to allocate resources in a router to multiple frames.

Wormhole:

Frames are divided into flits. The header flit contains the target addr. and it is used to reserve a path. Other flits just follow the path.



Head-of-Line (HOL)



The spread of blocking:

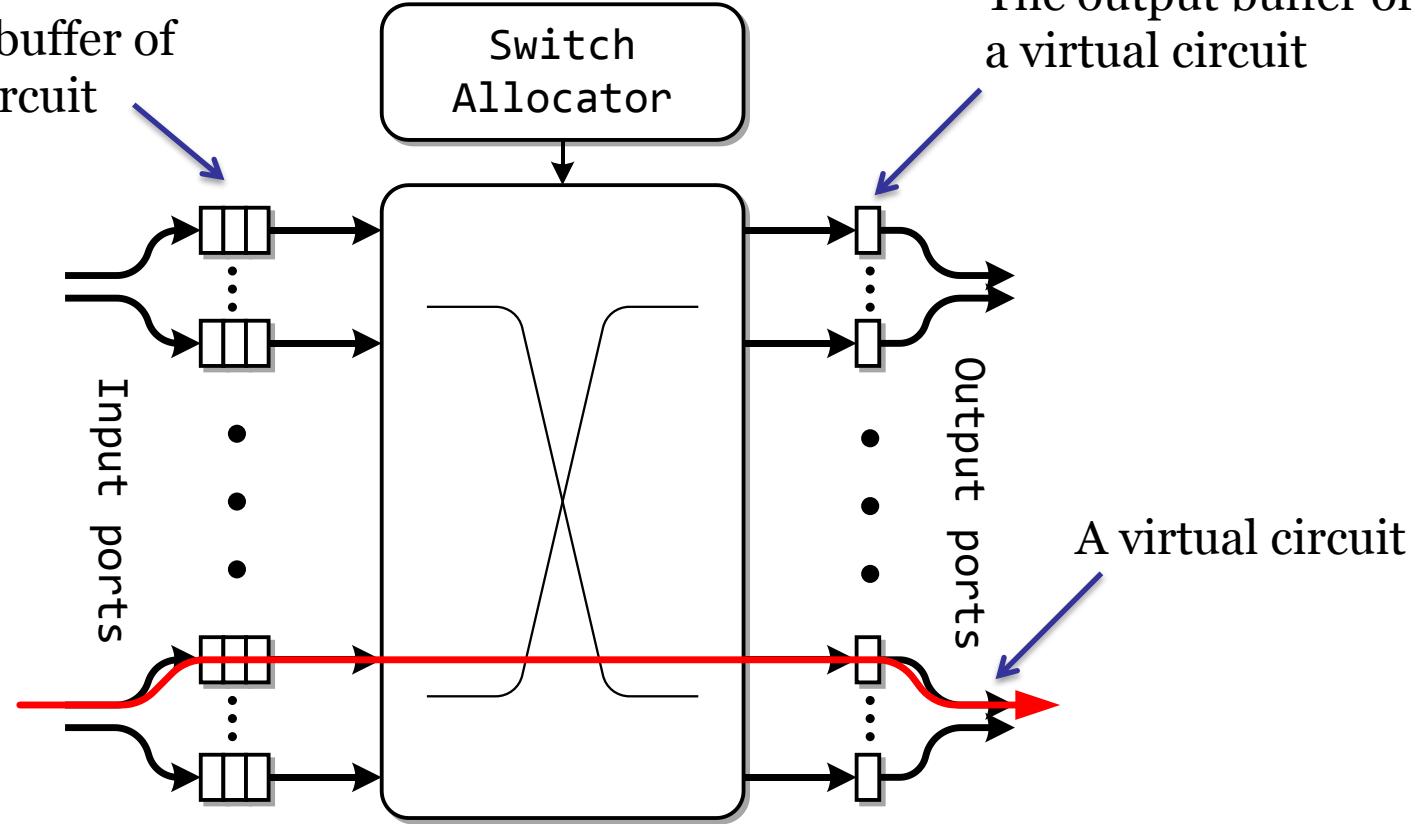
Assuming frame B is blocked by frame A, frame B may also block frame C; however, C is not directly related to A.

Spatial Division Multiplexing

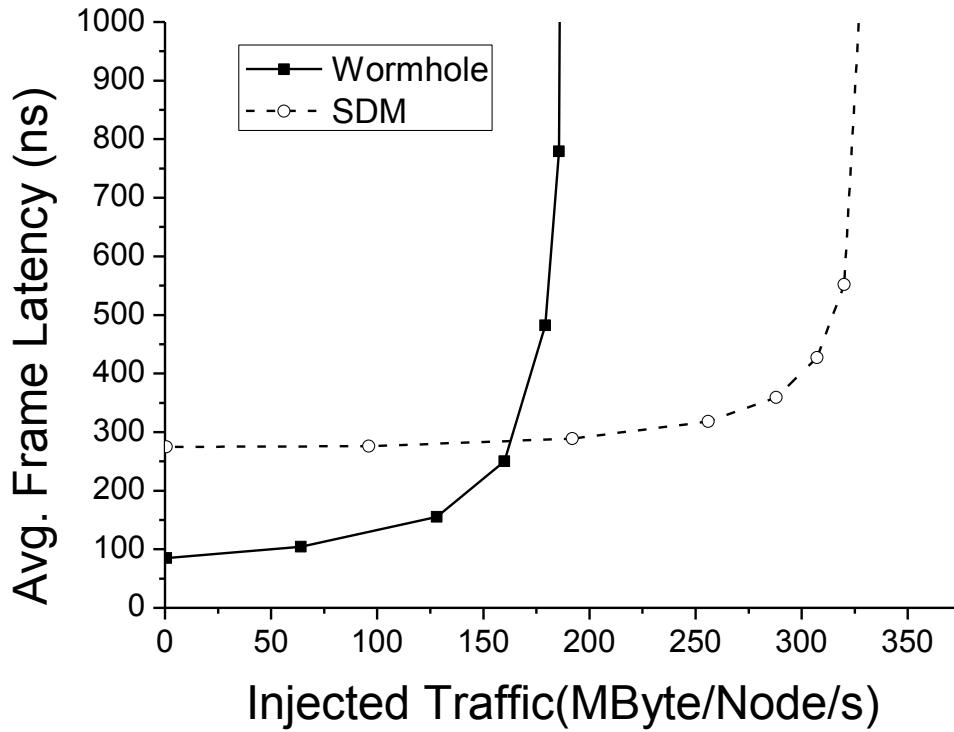
The input buffer of
a virtual circuit

Switch
Allocator

The output buffer of
a virtual circuit



SDM vs. Wormhole



	WH	SDM
Input Buf.	14,303	21,995
Output Buf.	5,935	6,000
Crossbar	4,356	21,744
Arbiters	772	22,208
Overall	25,366	71,956

The area of crossbars

WH:

$$P^*P^*W$$

SDM:

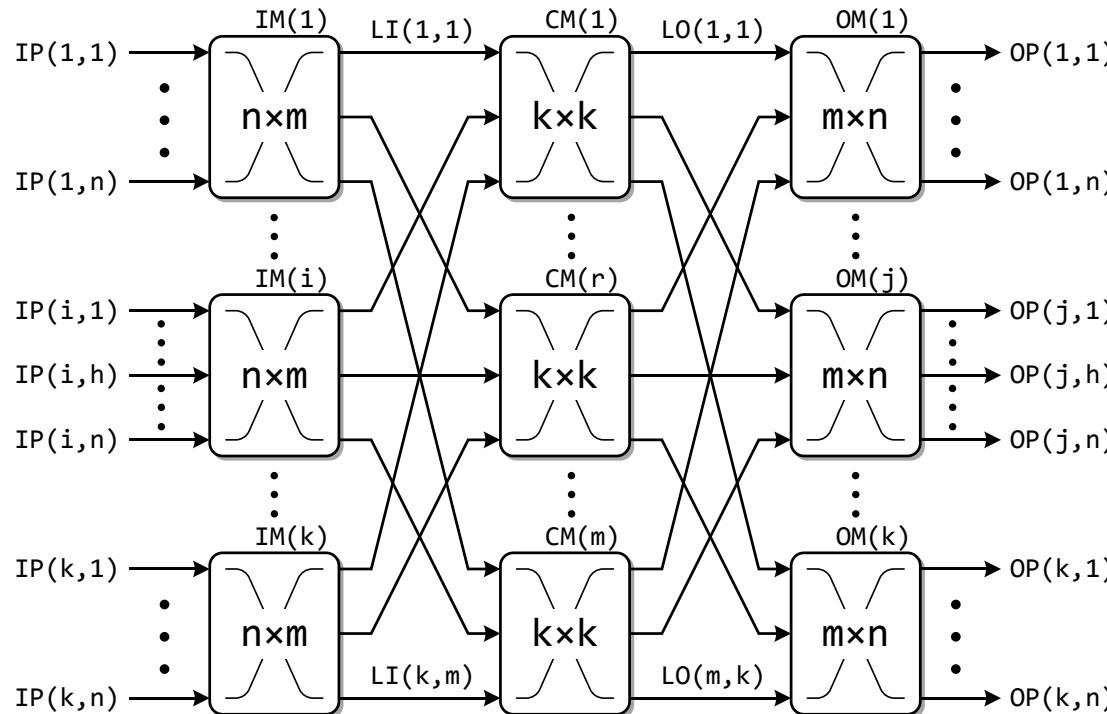
$$MP^*MP^*W/M = MP^*P^*W$$

[7] W. Song and D. Edwards. "Asynchronous spatial division multiplexing router," *Microprocessors and Microsystems*, 35(2), 85-97, 2011

Clos Switch - Motivation

- The problems of SDM
 - High-radix crossbars
 - Large crossbar and switch allocator
- Clos networks are the optimal switch structure
- Problems to solve
 - Dynamic configuration [11]
 - Optimal structure for SDM router (this paper)

Clos Networks



IP/OP: input/output port

IM: input module

CM: central module

OM: output module

n : number of IPs in IM

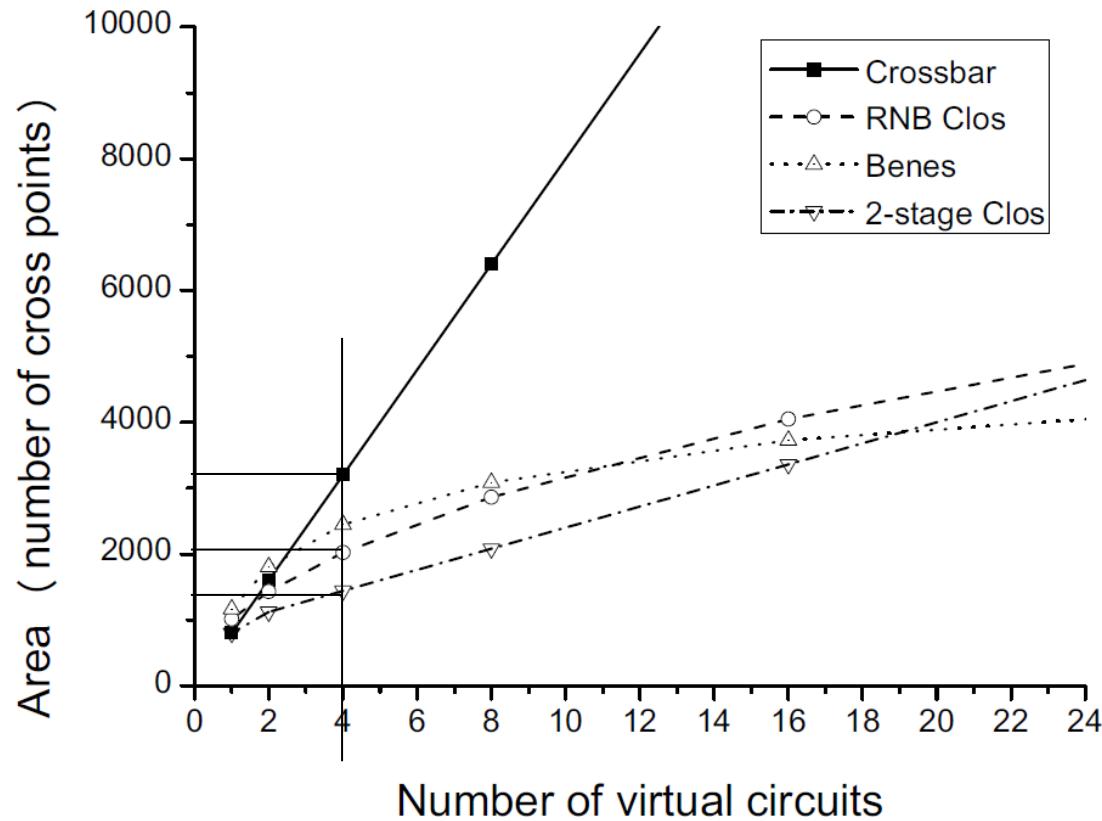
k : number of IMs

m : number of CMs

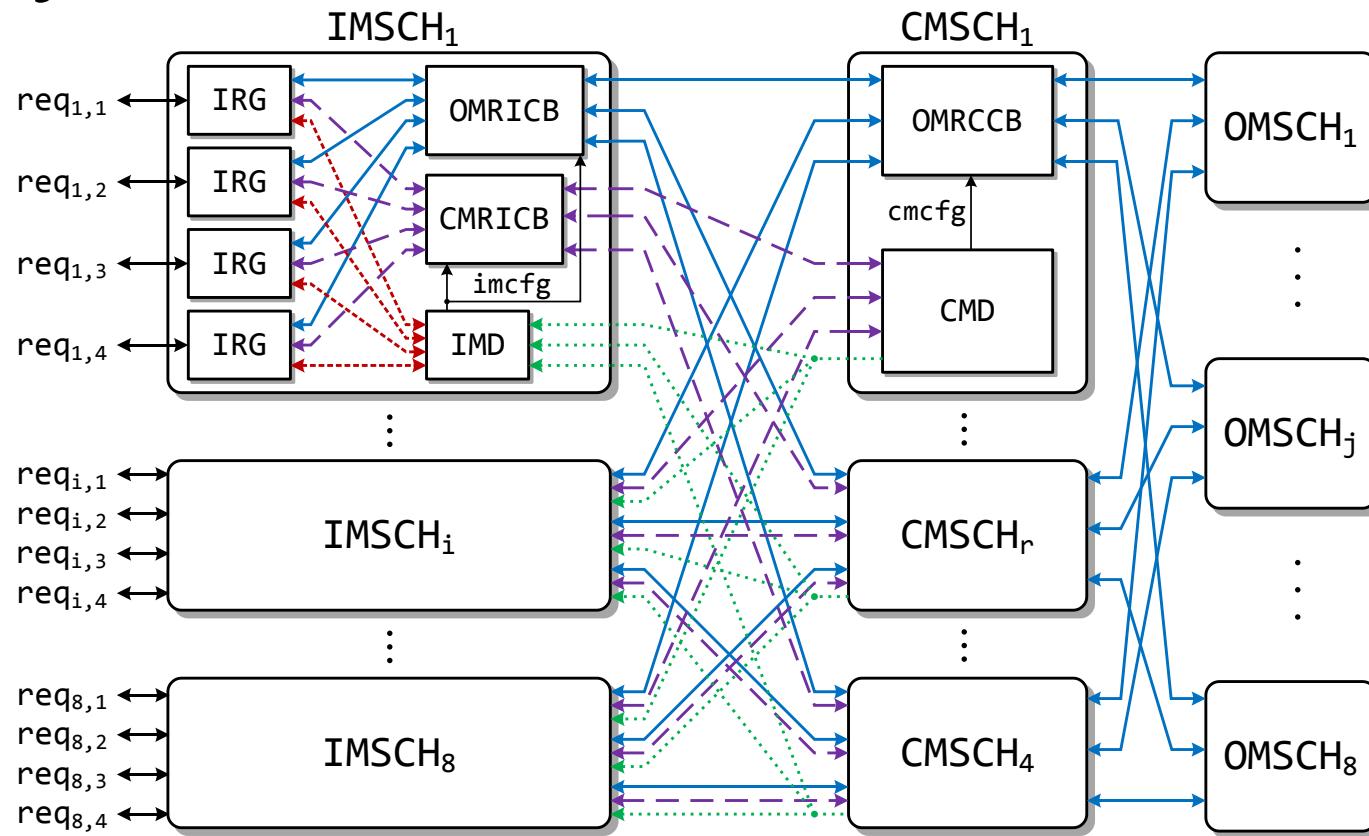
$N = kn$: the total number of IPs

When $m \geq n$, the switch is no-blocking

Clos vs. Crossbar

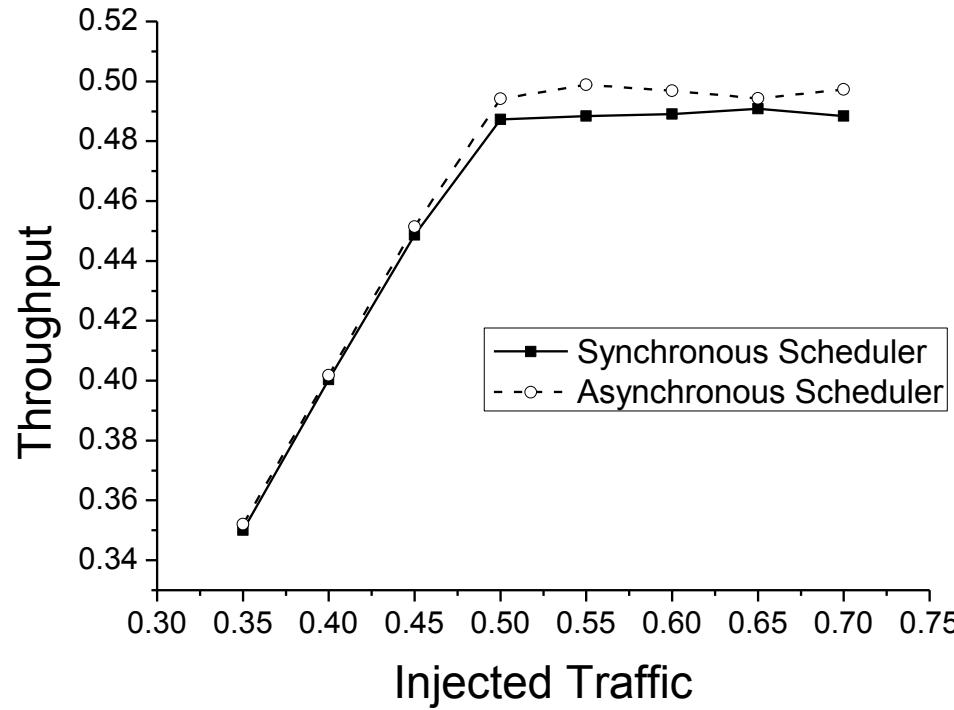


Asynchronous Clos Scheduler



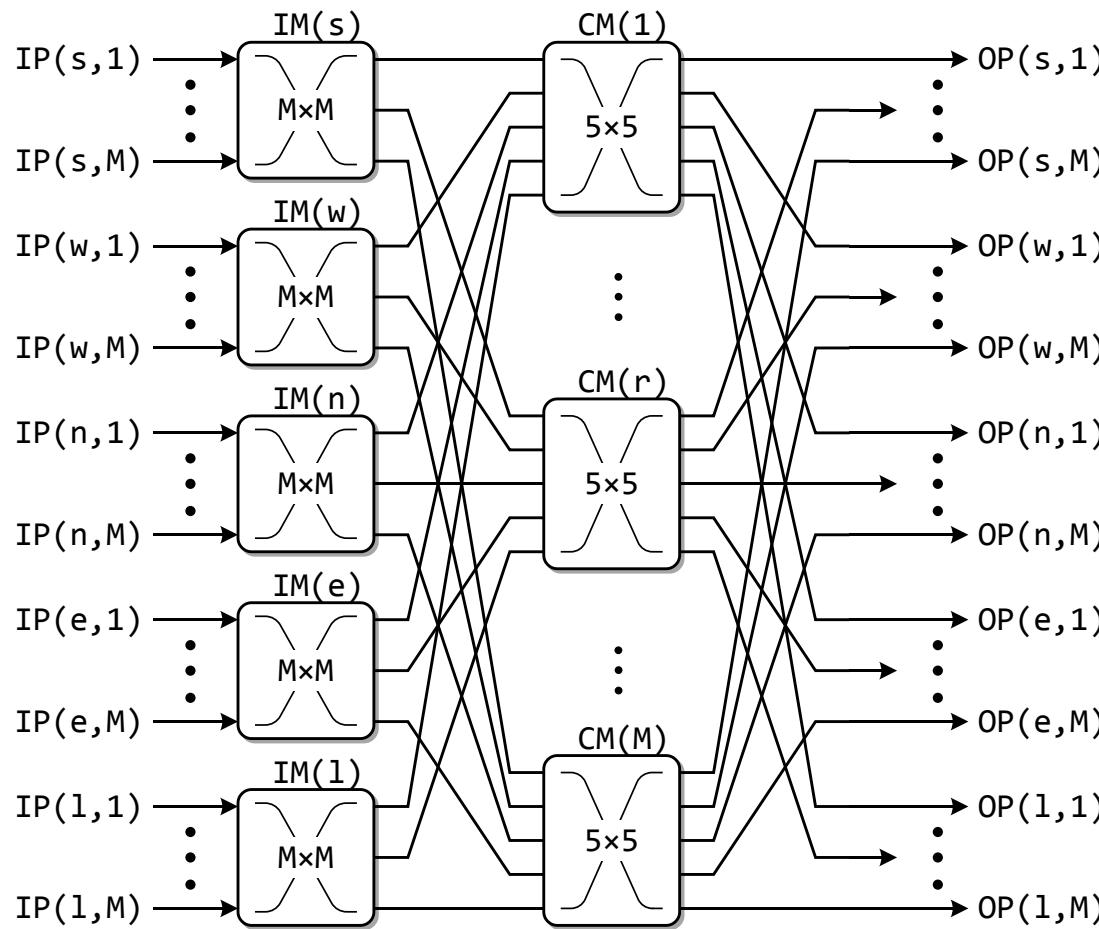
[11] W. Song and D. Edwards. “An asynchronous routing algorithm for Clos networks,” In *Proc. of International Conference on Application of Concurrency to System Design*, 2010, 67-76

Async vs. Sync Algorithm



[11] W. Song and D. Edwards. “An asynchronous routing algorithm for Clos networks,” In *Proc. of International Conference on Application of Concurrency to System Design*, 2010, 67-76

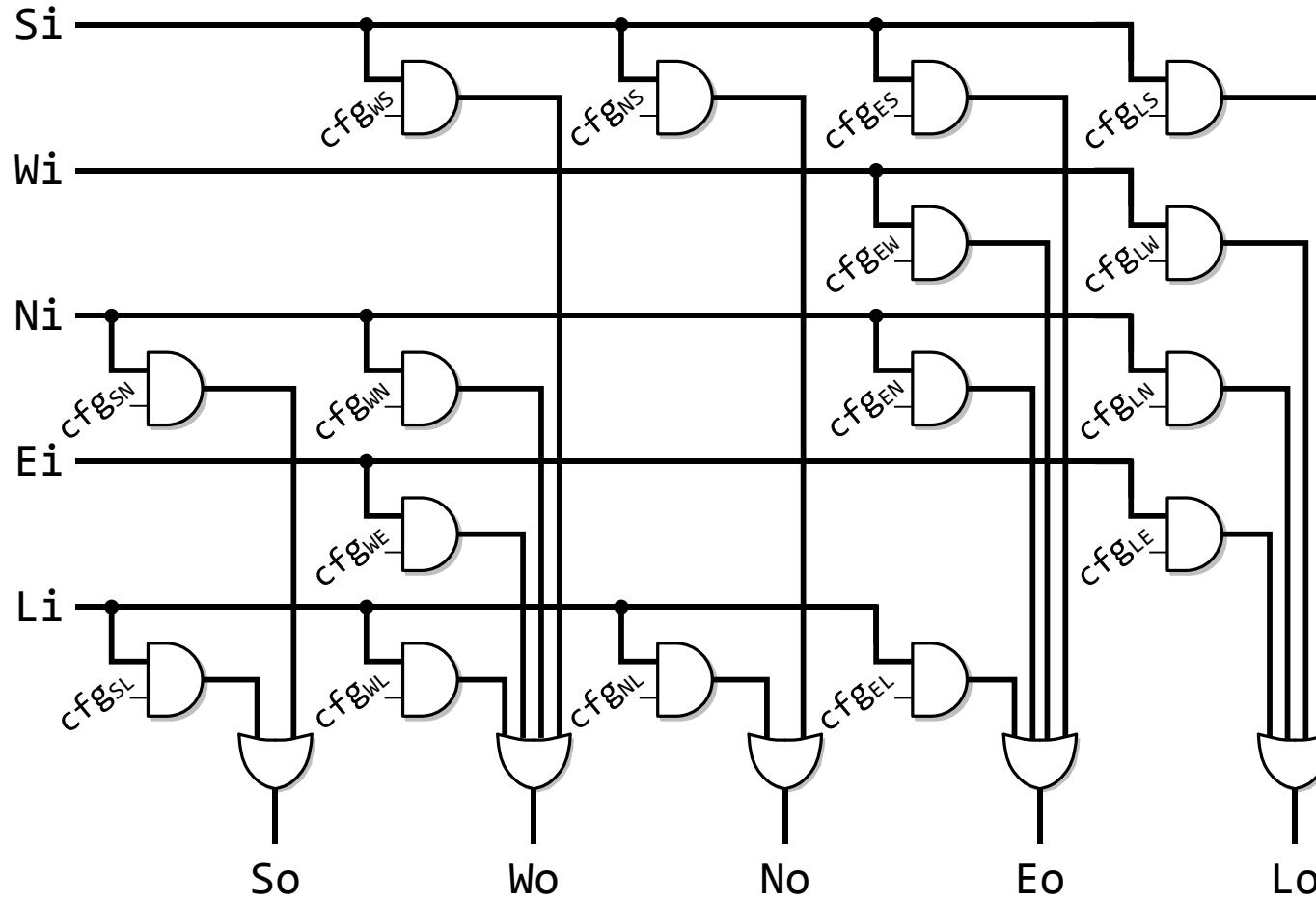
2-stage Clos Switch



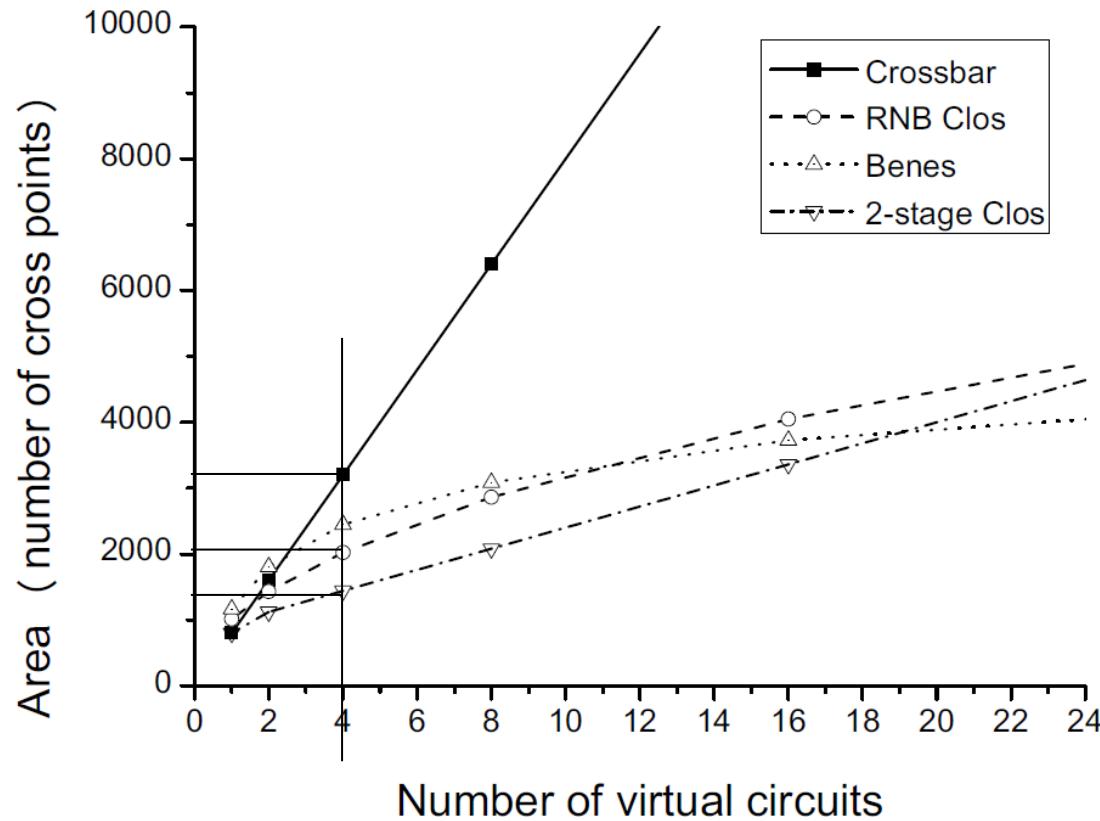
Benefits:

1. 2-stage
 - 1.a less latency
 - 1.b smaller
 - 1.c simpler scheduler
2. CMs can be further simplified

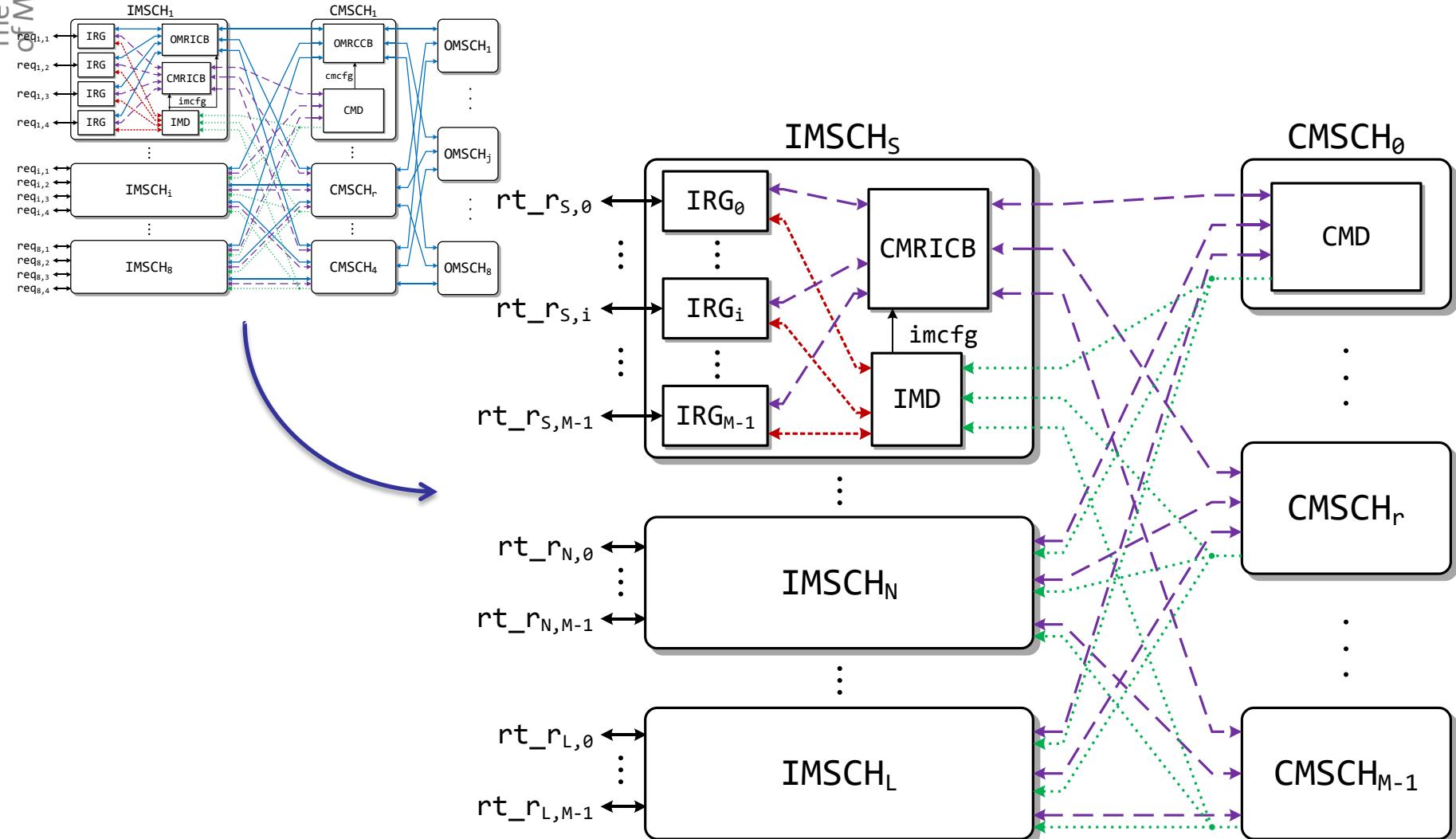
Simplified CM



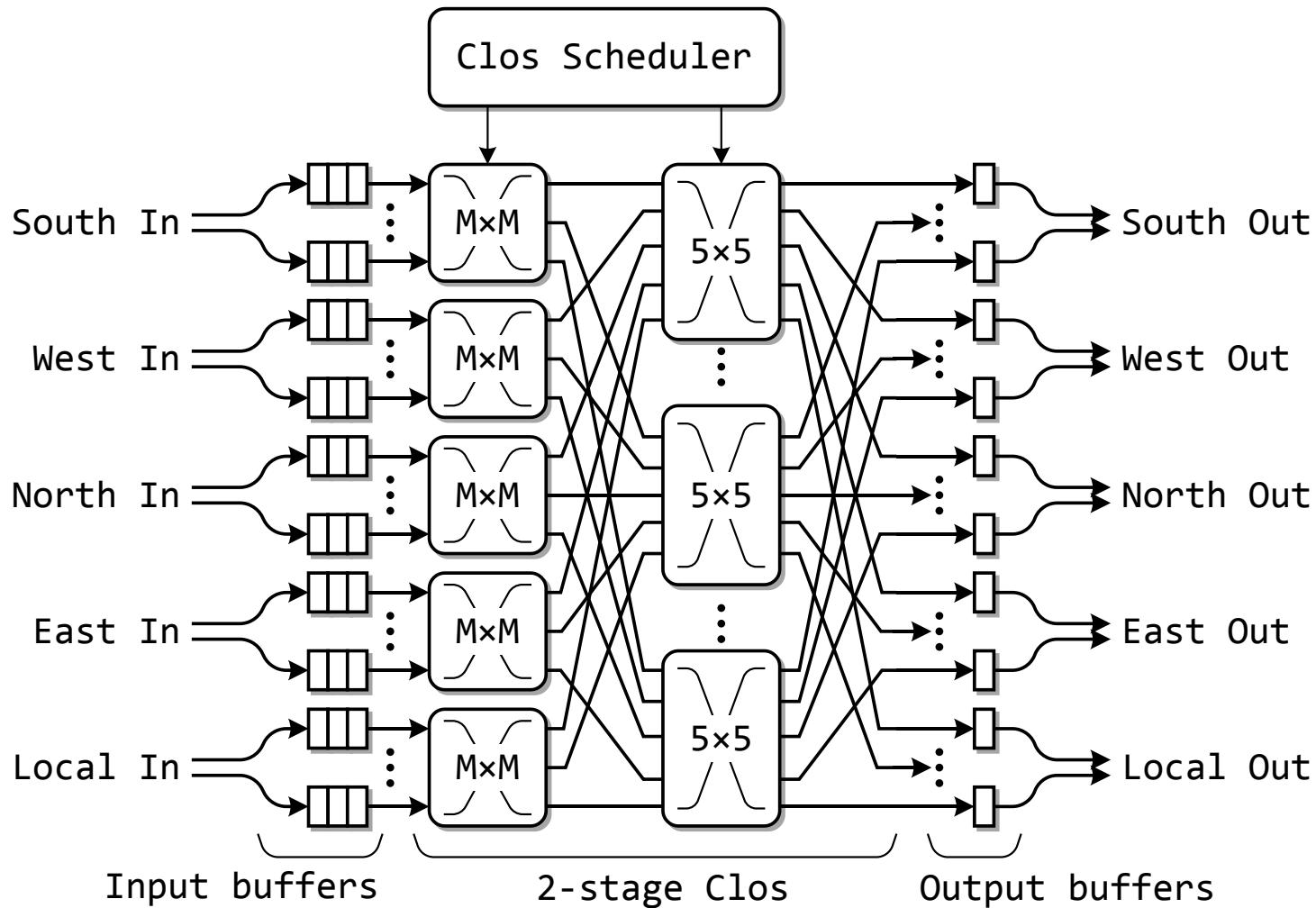
Clos vs. Crossbar



2-stage Clos Scheduler



A New SDM-Clos Router



Area Breakdown

	WH	SDM	SDM-Clos
IP Buf.	17,147	23,356	19,995
OP Buf.	11,034	9,016	8,893
Switch	17,754	69,701	33,417
Alloc.	909	83,485	19,884
Overall	48,170	187,872	84,054

(unit: μm^2)

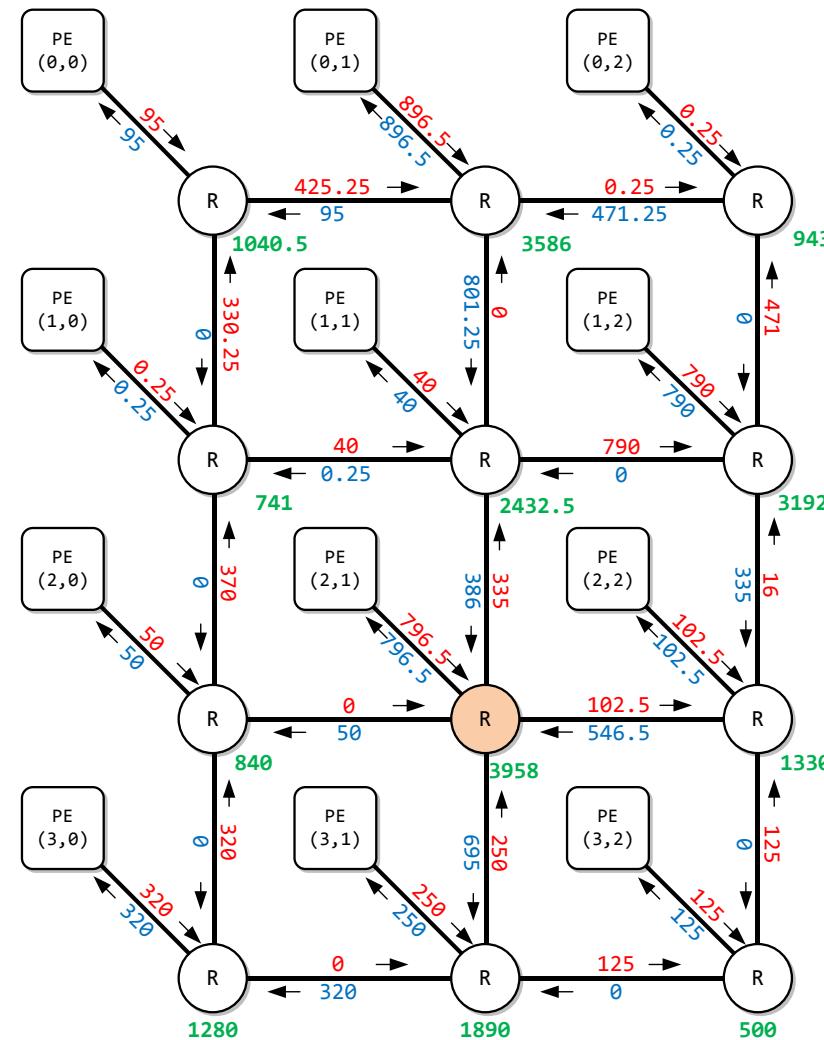
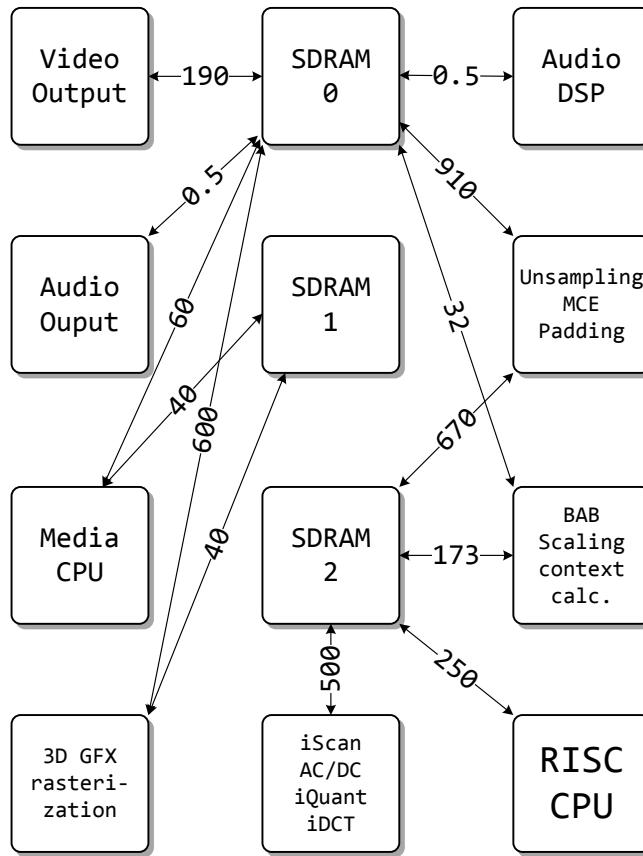
WH: 1 SDM: 3.9 SDM-Clos: 1.7

Speed Performance

	WH	SDM	SDM-Clos
Cycle period	2.24	2.86	2.67
Router latency	0.92	1.18	1.29
XY router	0.64	0.68	0.63
Allocation	1.24	2.01	2.13

(unit: ns)

Evaluation: MPEG-4



Network Performance

	WH	SDM	SDM-Clos
Throughput (MByte/s)	3414.6	3458.1	3458.1
Avg. latency (ns)	108.6	239.4	248.5
Power (mW)	15.6	15.2	13.6

Throughput requirement: ~3,400 Mbyte/s

SDM-Clos:

small latency overhead; low energy consumption; half of the area

Conclusion

- SDM improves throughput
- Clos switch can reduce the area overhead
- A new 2-stage Clos switch
 - Half area (4 virtual circuits)
 - Small latency overhead
 - Less energy consumption

Thanks

http://opencores.org/project,async_sdm_noc