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Asynchronous SDM Router

- results from ongoing research

Wei Song

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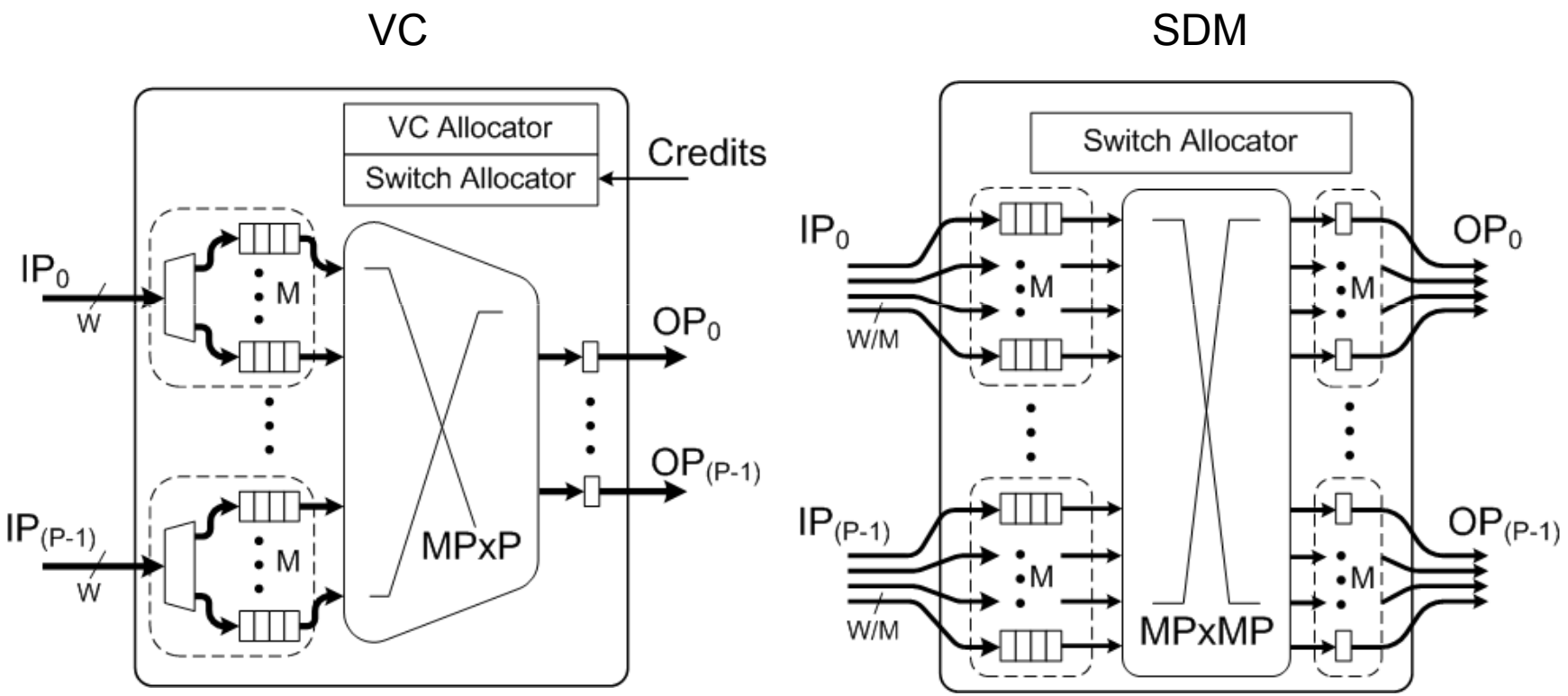
VC and SDM router



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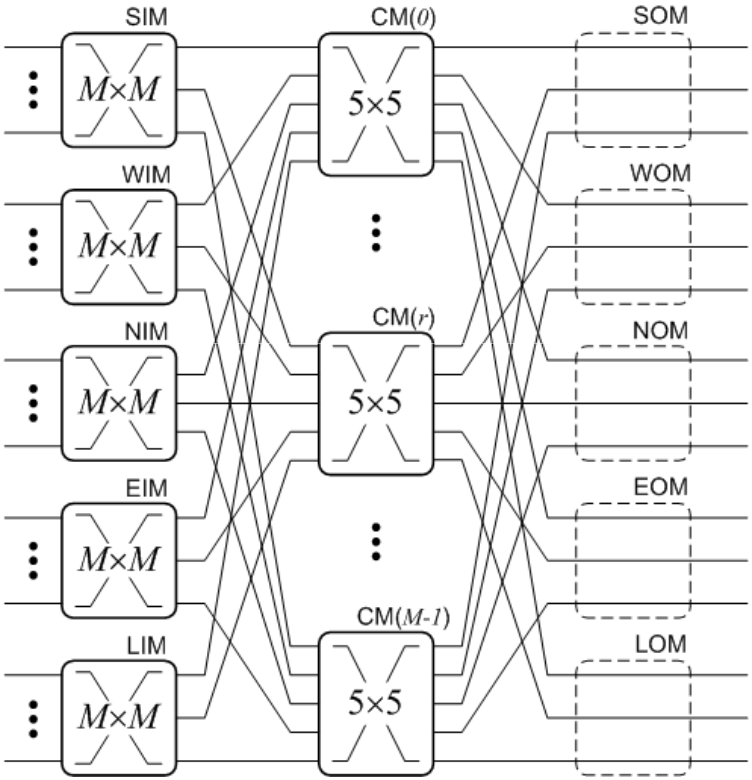
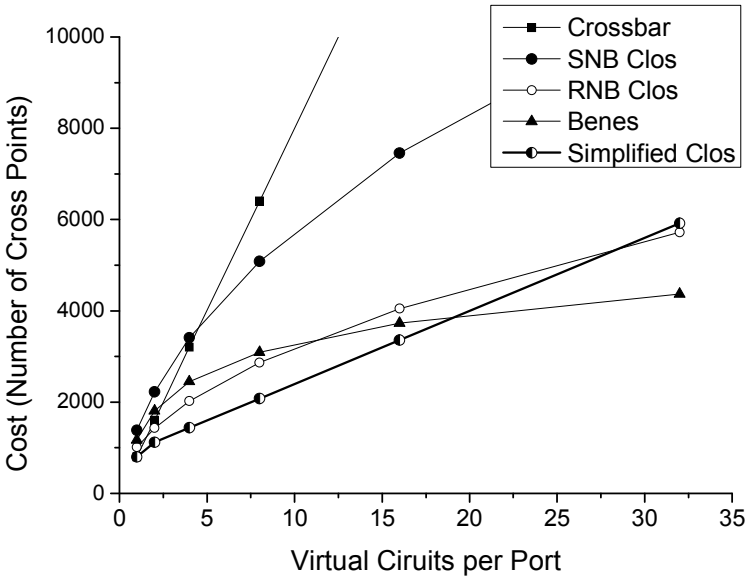
2-stage Clos Network





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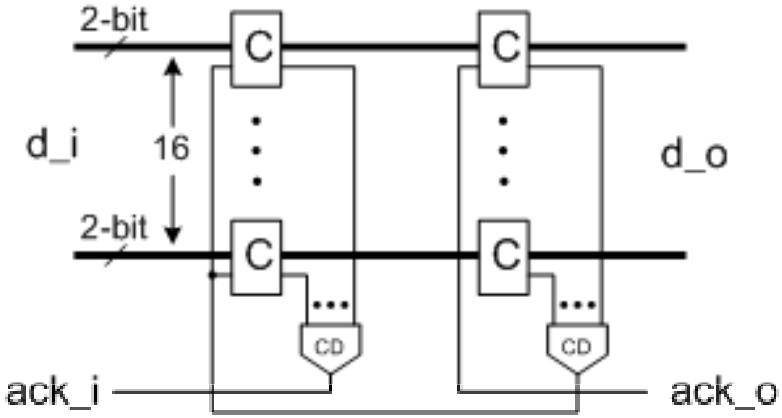
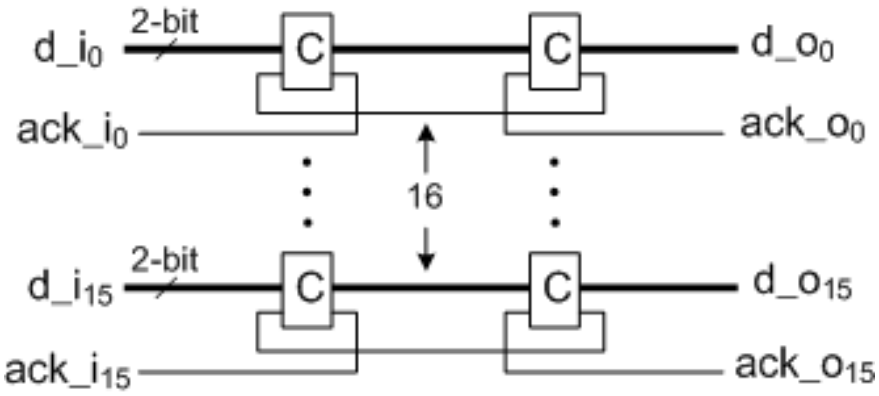
Channel Slicing





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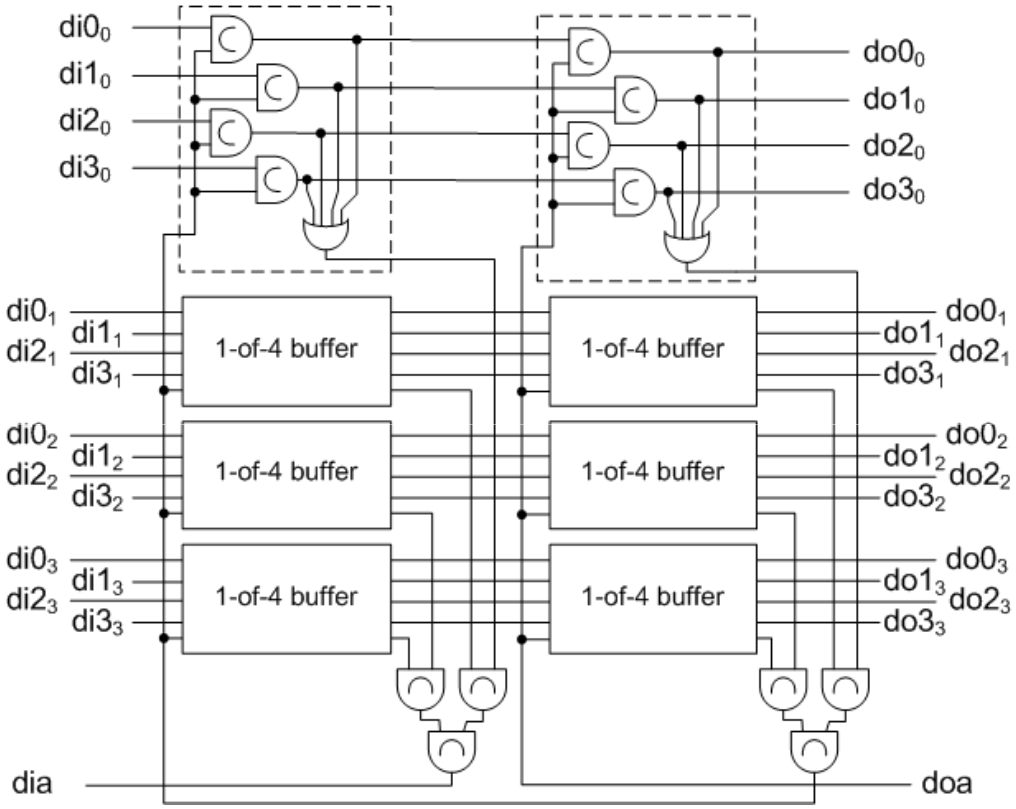
Questions from ASYNC'10

- Router Area: SDM vs. VC
- The area consumption of switch allocator
- Throughput: SDM vs. VC
- QoS support of SDM
- Wire efficiency on ports

- Area and latency models of Wormhole, SDM, and VC are extracted to answer these questions.

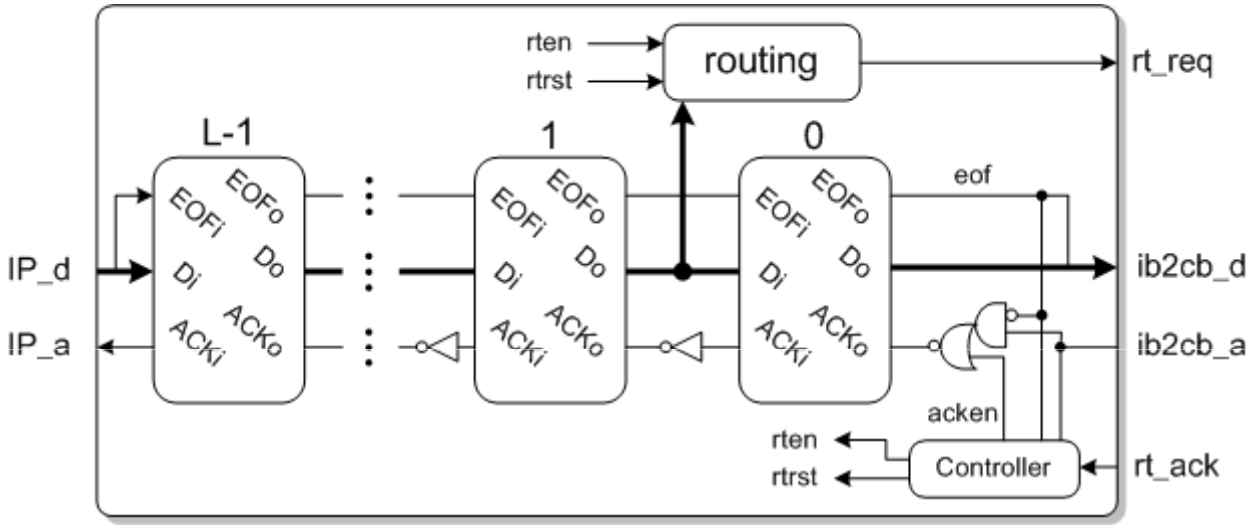
Area Model (1)



4-phase 1-of-4 QDI with common ACK

$$A_{pipe} = 2.5WA_C$$

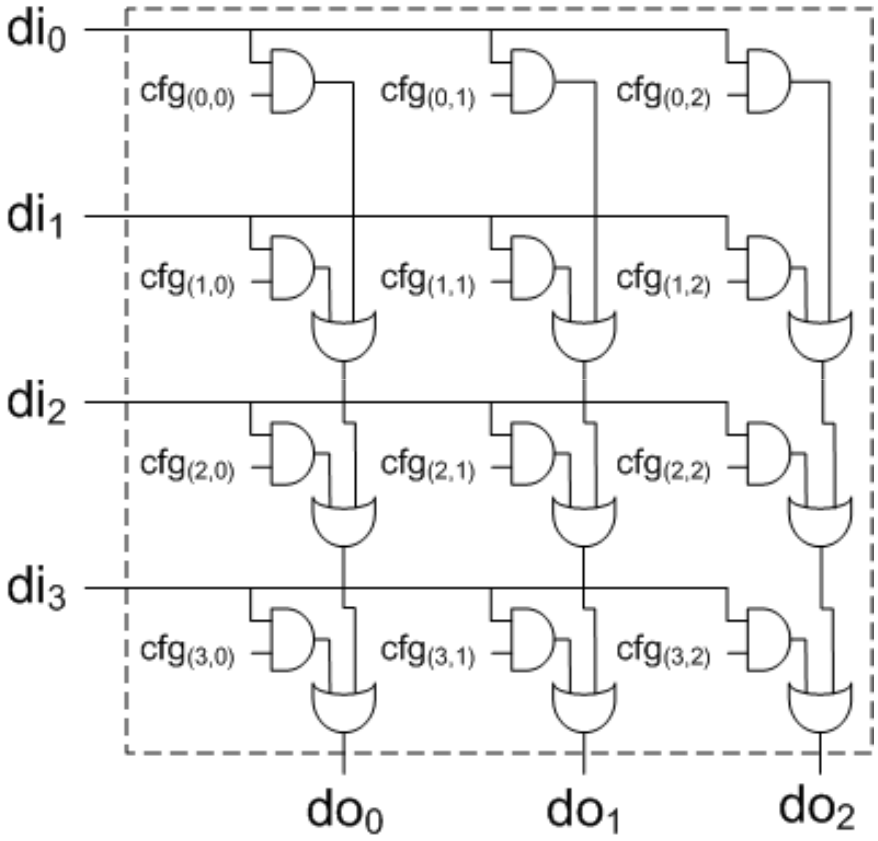
Area Model (2)



$$A_{IB,WH} = L(2.5WA_C + A_{EOF}) + A_{RC} + A_{CTL} \qquad A_{OB,WH} = 2.5WA_C + A_{EOF}$$

$$A_{IB,SDM} = M[L(2.5\frac{W}{M}A_C + A_{EOF}) + A_{RC} + A_{CTL}] \qquad A_{OB,SDM} = 2.5WA_C + MA_{EOF}$$

Area Model (3)

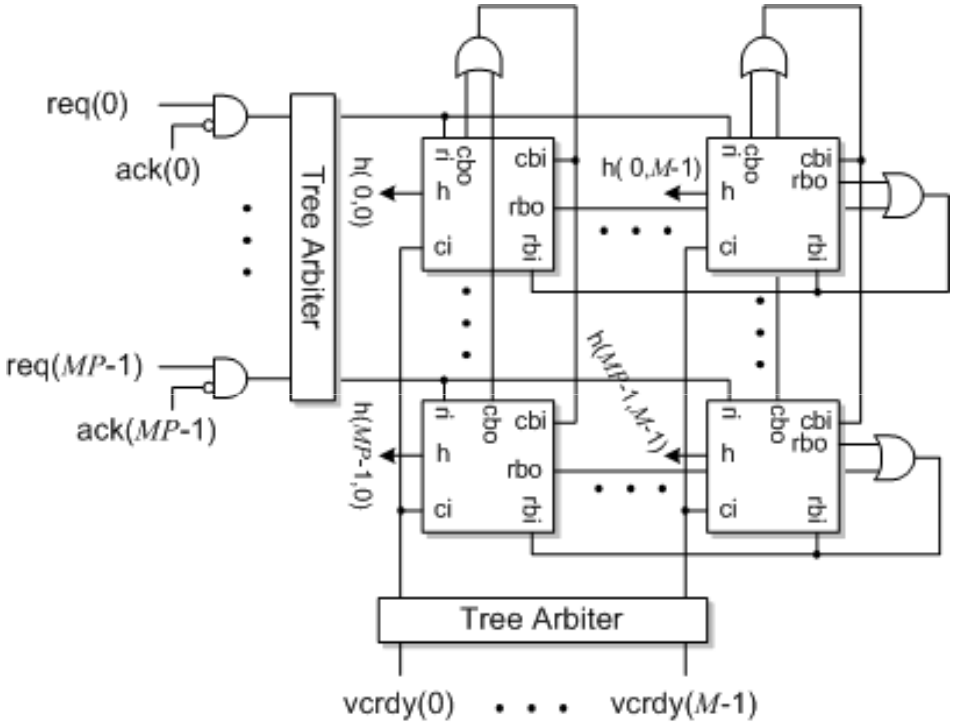


MxN crossbar includes
MN AND gates
(M-1)N OR gates

$$A_{CB,WH} = (2W + 2)(2P^2 - P)A_g$$

$$A_{CB,SDM} = (2\frac{W}{M} + 2)(2M^2P^2 - MP)A_g$$

Area Model (4)



$$A_{A,WH} = P^2 A_{arb}$$

$$A_{A,SDM} = M^2 P^2 A_{arb}$$

MxN multi-resource arbiter
Includes MN tiles

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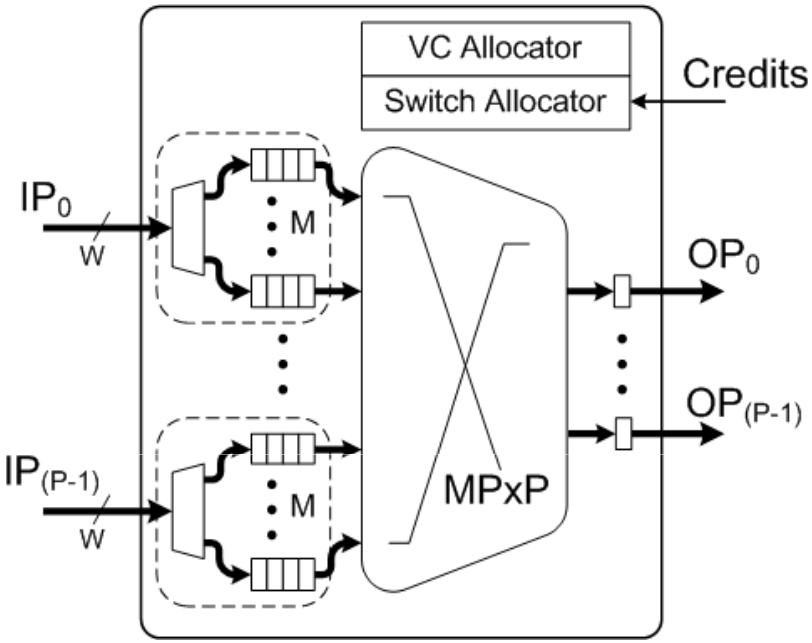
Area Results

Table 1: Area consumption (μm^2)

	WH	err(%)	SDM	err(%)	SDMCS	err(%)
Input Buffers	14,303	0.0	21,995	-0.4	25,953	-0.1
Output Buffers	5,935	0.0	6,000	1.7	6,540	3.4
Crossbar	4,356	0.0	21,744	-0.2	28,992	-0.2
Switch Allocator	772	78.2	22,208	-0.9	22,122	-0.5
Total	25,366	2.4	71,956	-0.3	83,615	0.0

P=5, L=2, W=32, M=4

Area of VC routers



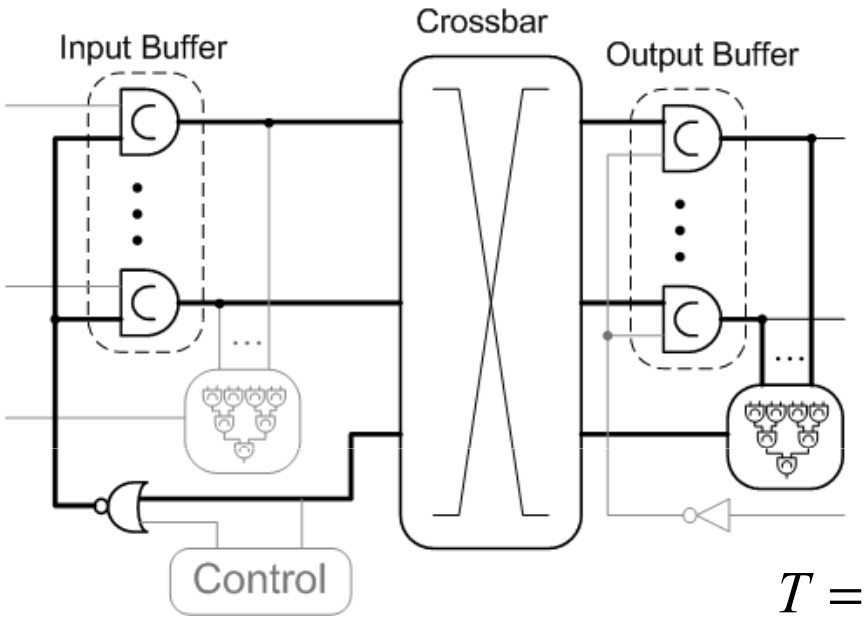
$$A_{IB,VC} = M \cdot A_{IB,WH} \approx M \cdot A_{IB,SDM}$$

$$A_{OB,VC} = A_{OB,WH} \approx A_{OB,SDM}$$

$$A_{CB,VC} = (2W+2)(2MP^2 - P)A_g \approx A_{CB,SDM}$$

$$A_{A,VC} = (M^2P^2 + P^2)A_{arb} = A_{A,SDM} + A_{A,WH}$$

Critical Cycle Analysis



$$T = 4t_C + 4t_{CB} + 2t_{CD} + 2t_{AD} + t_{CTL}$$

$$t_C = l_C + k_C \cdot N_{CB\_O}$$

$$t_{CB} = l_{CB} + k_{CB} \cdot \log_2 N_{CB\_O}$$

$$t_{CD} = l_{CD} + l_C \cdot N_{CD\_depth} + k_{CD} \cdot N_{CB\_I}$$

$$t_{AD} = l_{AD} + k_{AD} \cdot N_{wire\_count}$$

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Speed Performance

	WH	err	SDM	err	SDMCS	err	VC
Period	4.25	2.6	4.15	-3.4	3.12	3.8	5.23
Latency	2.29		2.49		2.66		N/A
Routing	0.44		0.51		0.50		0.44
Allocation	0.78		3.21		3.28		3.21
t_C	0.22	-9.1	0.34	-5.9	0.29	10.3	0.20
t_{CB}	0.16	1.3	0.26	-3.8	0.24	4.2	0.16
t_{CD}	0.79	7.6	0.57	4.2	0.30	-2.0	0.89
t_{AD}	0.57	6.1	0.27	-0.4	0.17	8.8	0.61
t_{CTL}	0.00		0.00		0.00		0.78

Unit: *ns*

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Simulation Configuration

- Latency accurate SystemC models
- Wormhole, SDM, SDM+CS, VC
- 8x8, 5 ports, XY routing
- 32-bit, 4 VCs/virtual circuits

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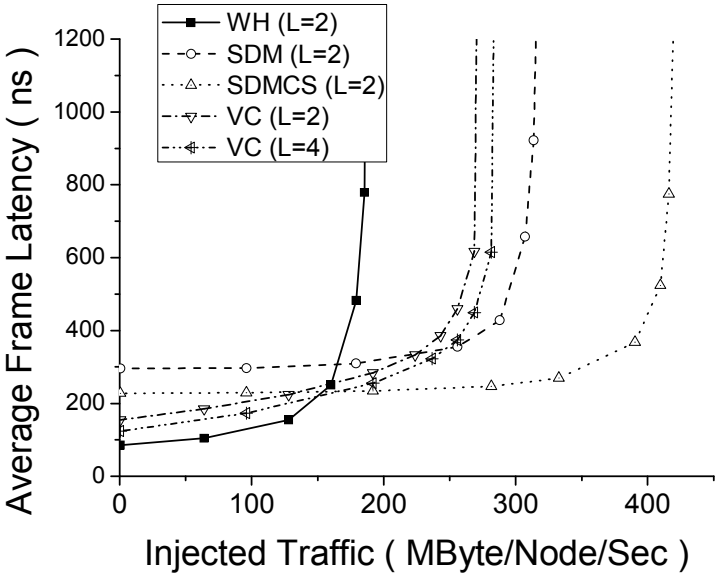
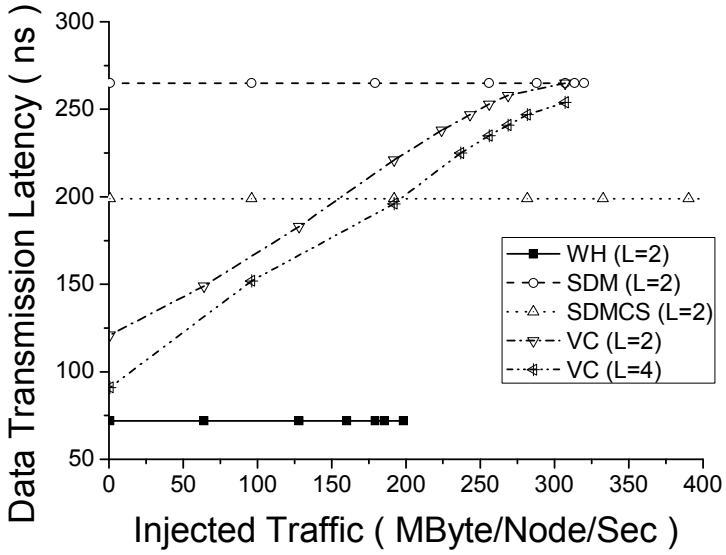
Injected Traffic vs. Latency





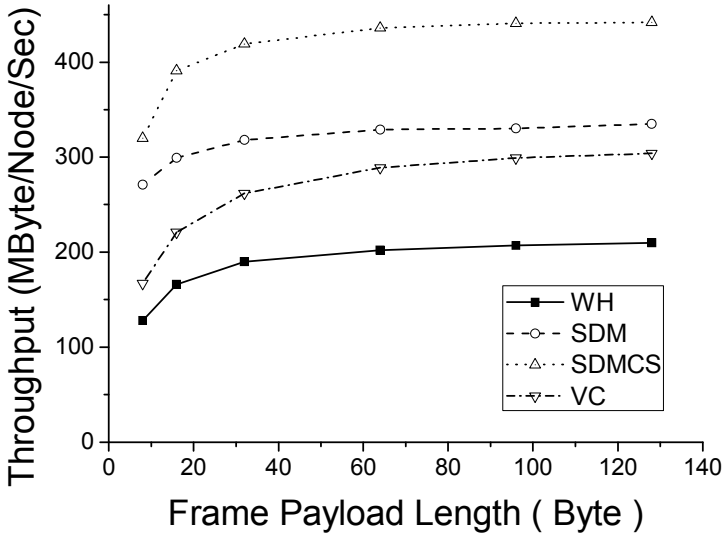
L=2, W=32, FL=64

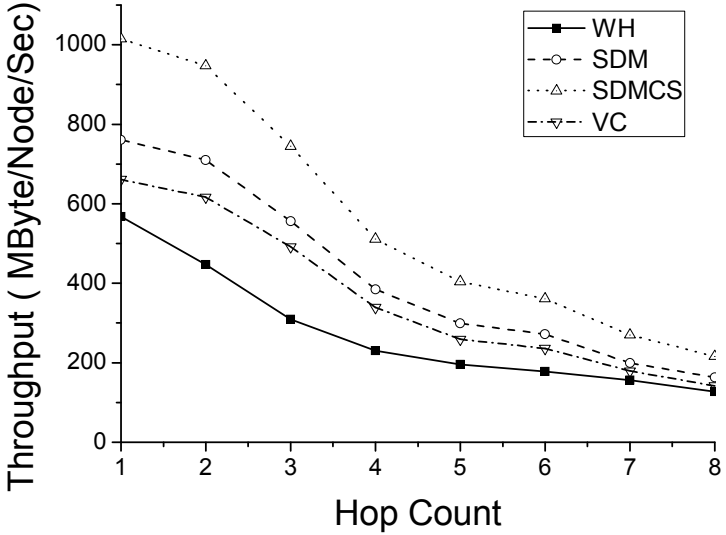
VC router with L=2 suffers from credit loop stall.

Both SDM and SDMCS outperform VC.

Wormhole, SDM and SDMCS have constant data transmission latency.

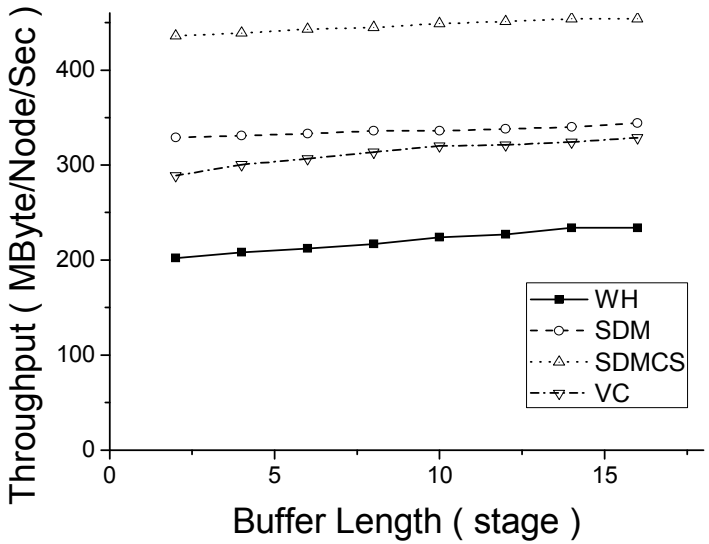
Payload and Hop Count

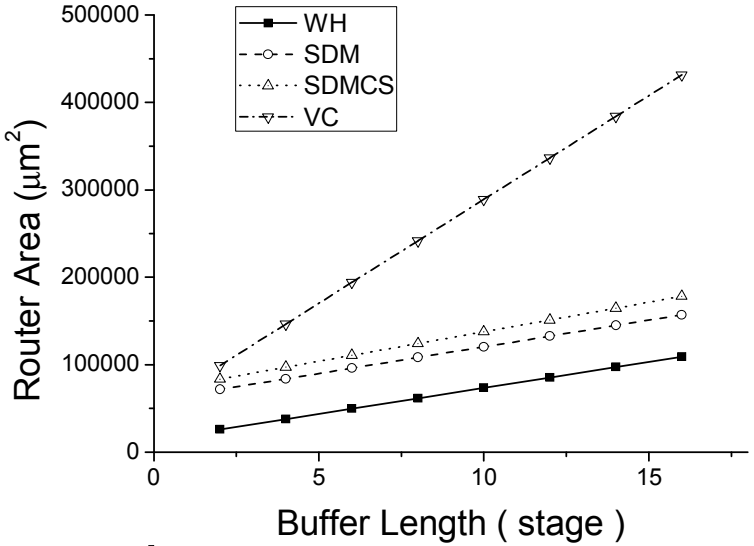




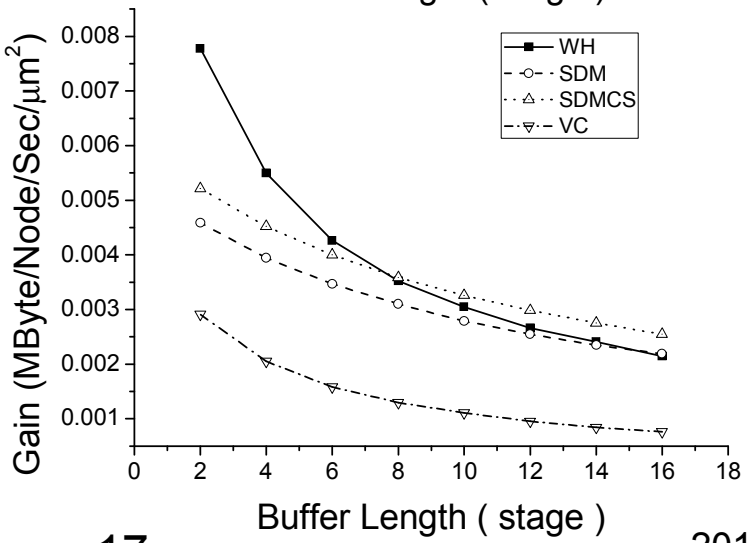
All routers approach the maximal throughput with longer payload length.
FL=64 Byte shows 90% maximal throughput.
Throughput decreases with the increasing hop count.
SDM shows better through even in the 8-hop case.

Buffer Length

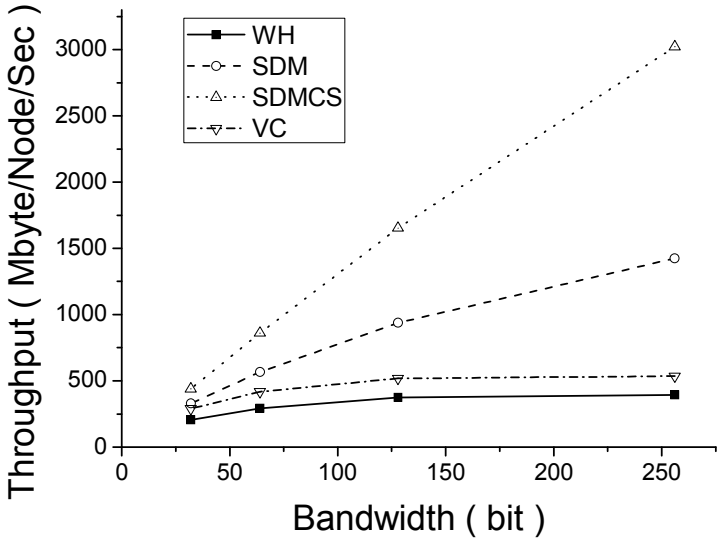


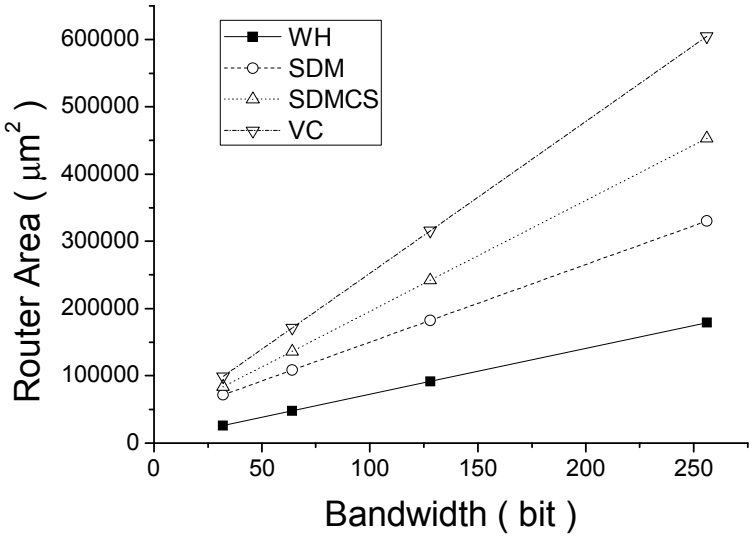


$$Gain = \frac{Throughput}{Area}$$

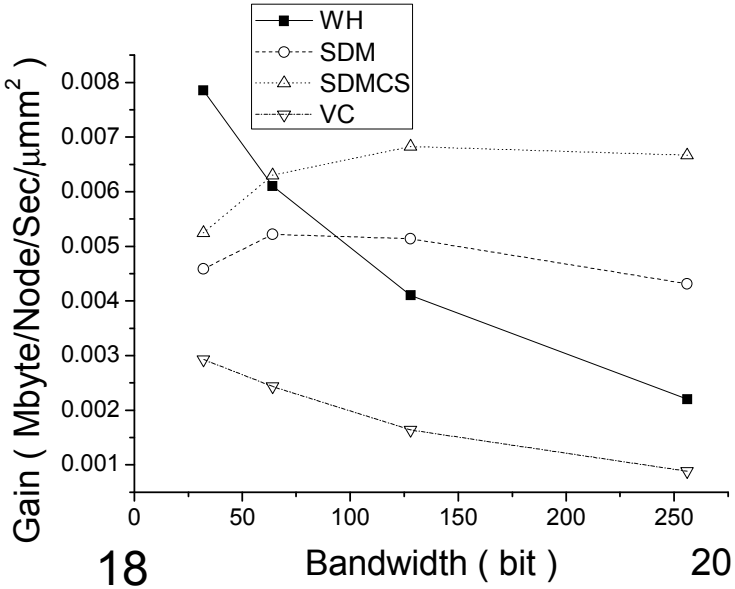


Bandwidth





$$Gain = \frac{Throughput}{Area}$$



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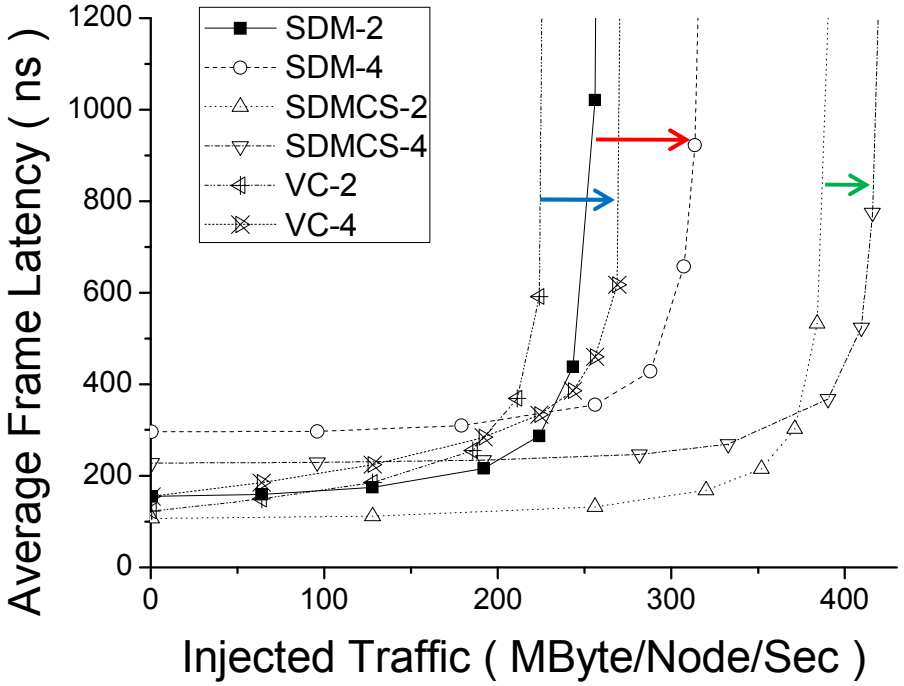
Number of VCs/Virtual Circuits



- Throughput increment from 2VC to 4VC
  - VC 20% SDM 22.5% SDMCS 6.7%

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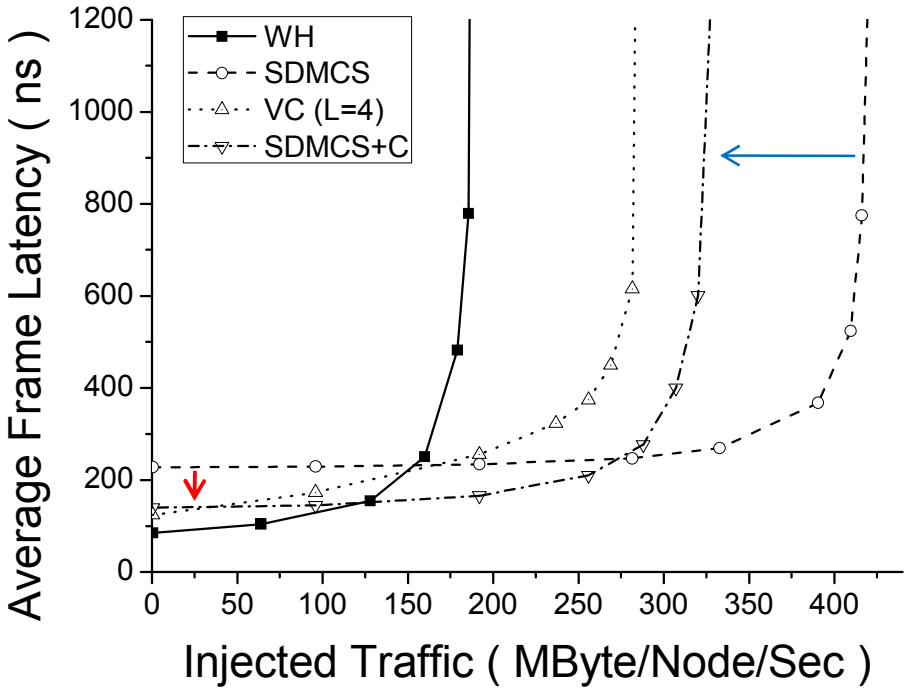
Reduce the latency



- The frame latency can be reduced significantly if a frame is divided and delivered by two virtual circuits concurrently.

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Port Wire efficiency

- Wormhole $\rho_{WH} = \frac{W}{2W+2}$ 48.5%
- SDM $\rho_{SDM} = \frac{W}{2W+2M}$ 44.4%
- SDMCS $\rho_{SDMCS} = \frac{W}{3W} = \frac{1}{3}$ 33.3%
- VC $\rho_{VC} = \frac{W}{2W+3+2M}$ 42.7%

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Conclusion

- SDM+CS achieves the best performance and the best Gain (except wormhole) for best-effort traffic.
- SDM+CS has smaller area than VC with the same configuration.
- SDM has the potential ability to support hard delay guaranteed services.

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Ongoing Work

- The VC designed by Tomaz Felicijan (QoS Router) has been implemented again.
- Prove the throughput improvement by probability theories.
- Estimate the theoretical throughput bound of the 2-stage Clos network and optimize it.
- Reduce the area consumption of the Clos allocator.

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Thanks! Question?