MANCHESTER 1824

The University of Manchester

A Wormhole Router Design

progress report

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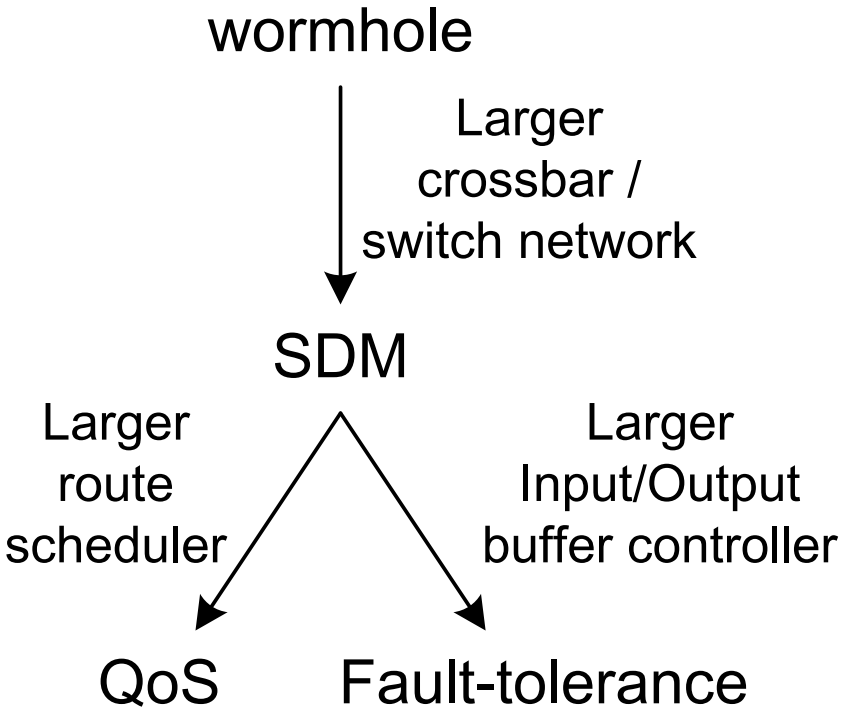
Content

- Motive and Plans
- Wormhole router
  - Channel Slicing, motivation
  - Lookahead, critical cycle
  - Implementation
- XY/Stochastic routing scheme

Why a wormhole router now

- Easy
- Smallest cycle period
- Early performance estimation
- Proof of channel slicing



Plan for Router Design (1)

- Wormhole router
  - Speed estimation, basic design flow
  - Channel slicing, lookahead pipeline
- Spatial Design Multiplex (SDM) router
  - Utilizing channel slicing (provide virtual circuit)
  - *M* sub-channels on a port, crossbar**M*
  - Benes, Clos switch network (ATM)
  - Route scheduling in the multi-stage switch

Plan for Router Design (2)

- Dynamic Link Allocation
  - Allocate idle sub-channels to active virtual circuits to reduce frame latency
  - Arbitration planning, crossbar reconfiguration and buffer planning
- Fault-tolerance
  - Error detection, deadlock recovery, route scheduling algorithm

Plan for Router Design (3)

- QoS
  - Virtual circuit is latency and bandwidth guaranteed (weak if dynamic link allocation is used)
  - Best Effort is a problem
  - Priorities for virtual circuit setup (reduce circuit setup time for high priority services)

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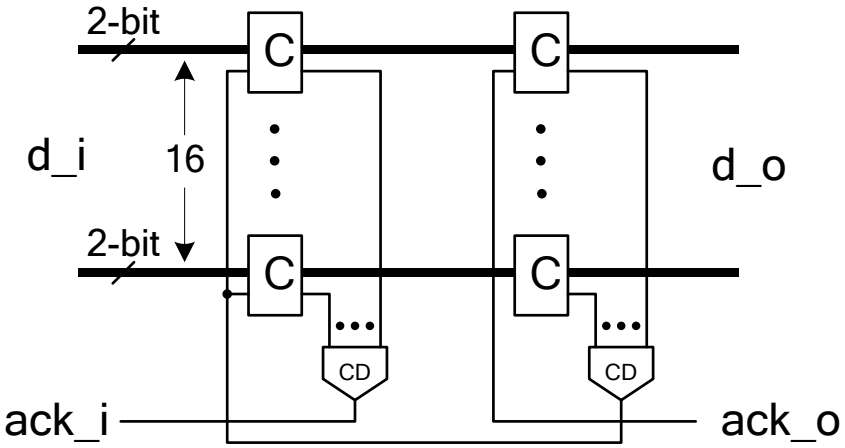
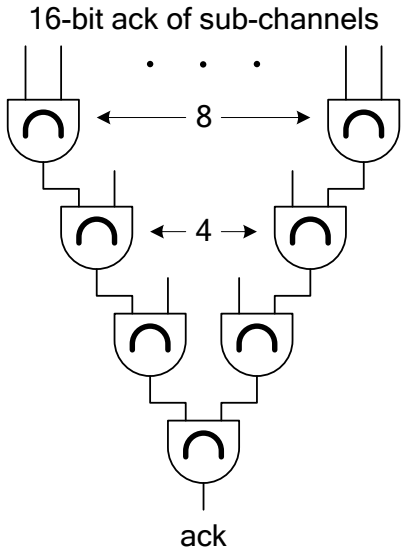
ChSlice: motive

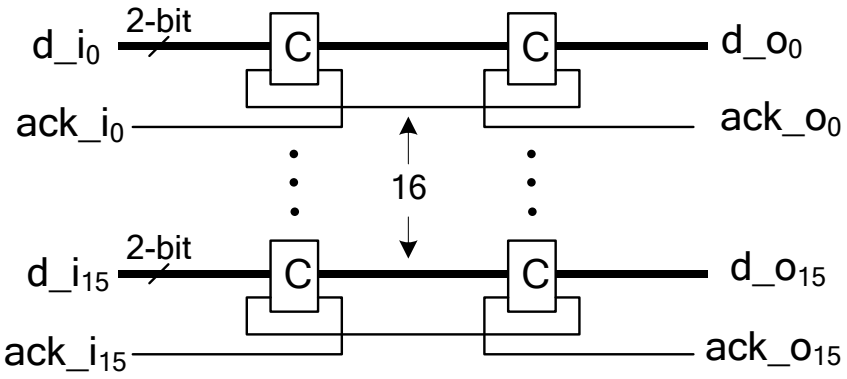


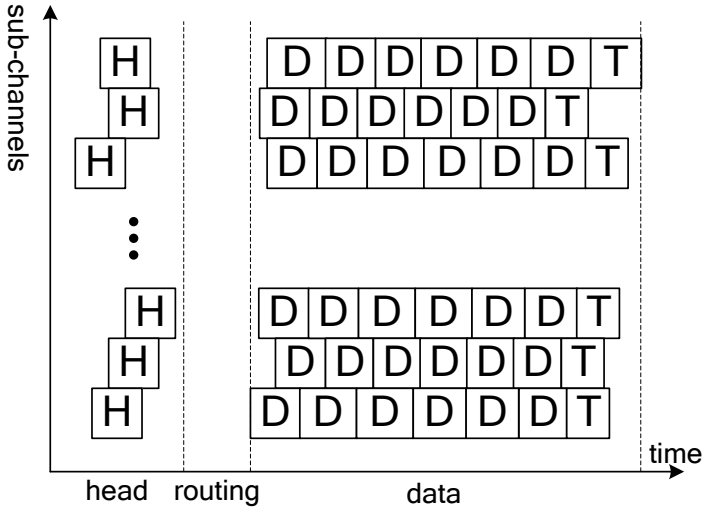


Advantages: data on all sub-channels are synchronized, ease the time division multiple access (TDMA) techniques, such as virtual channel and TDMA

Drawbacks: low speed (66% on CD)

ChSlice: implementation





ChSlice: conclusion

- Advantage
  - fast
- Overhead
  - extra controllers
  - larger wire-count

- No *TDMA* techniques but *SDM* is easy.

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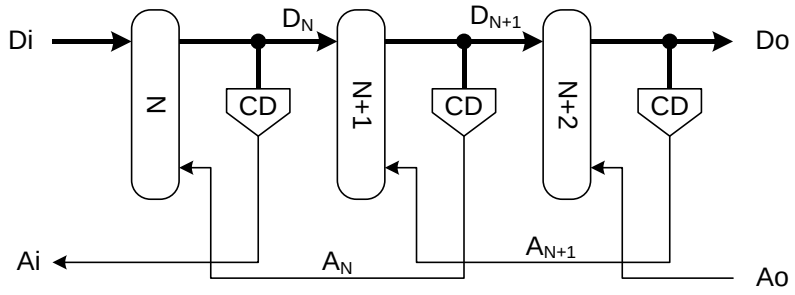
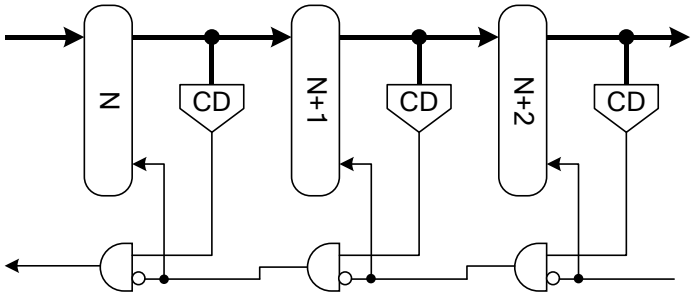
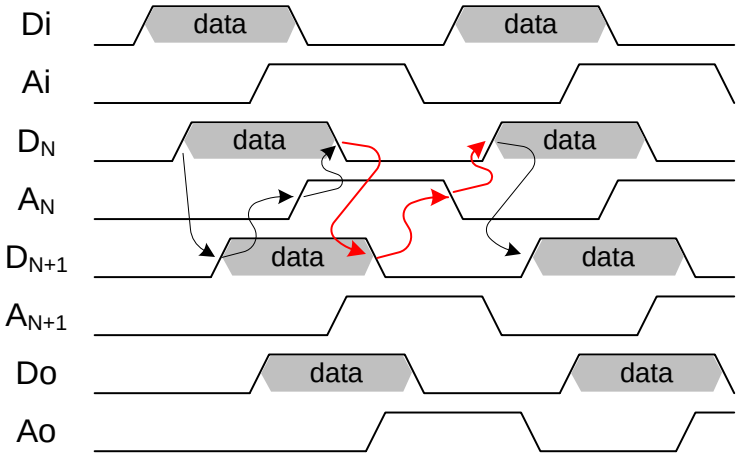
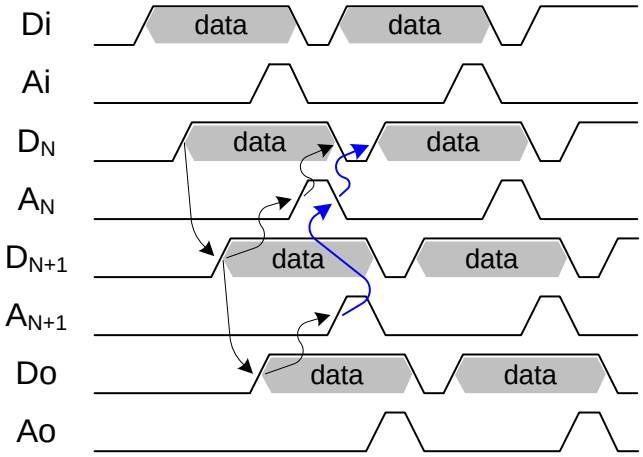
Lookahead: pipeline style



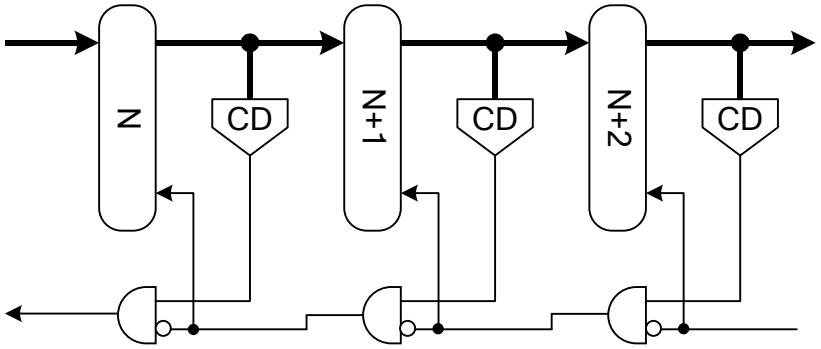


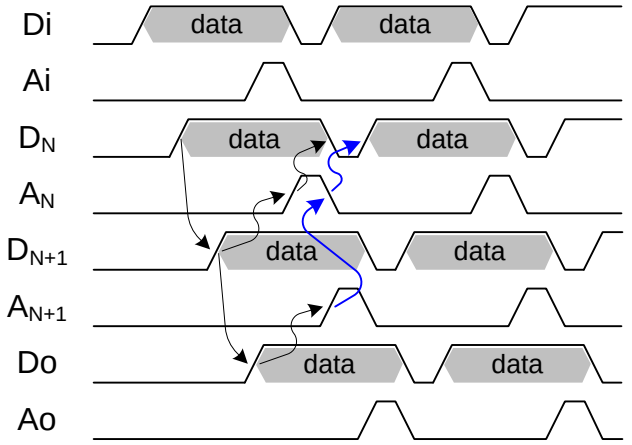




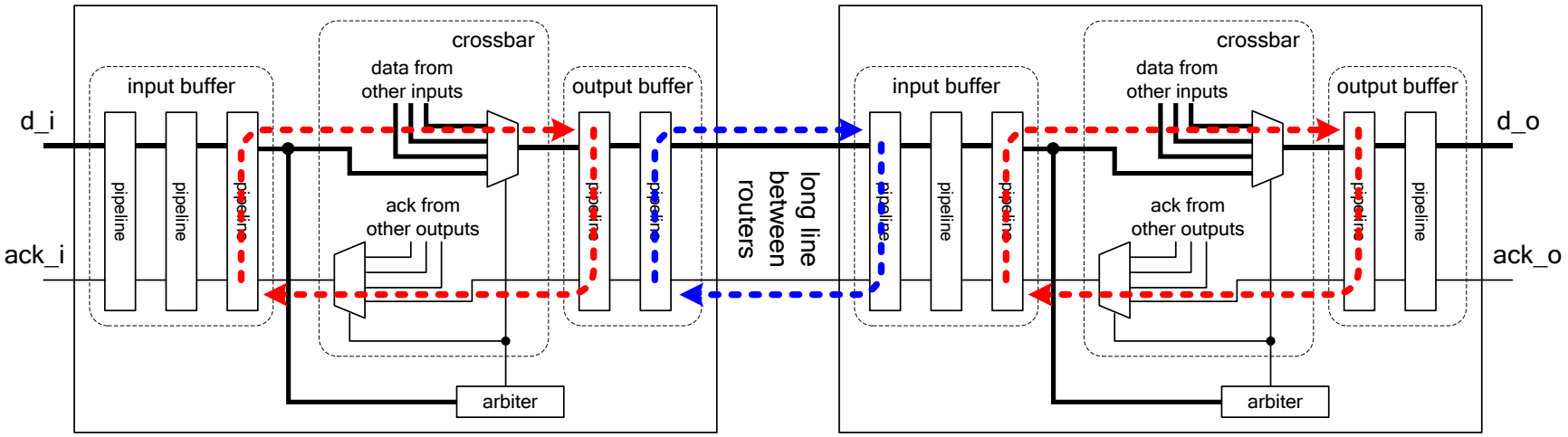
Lookahead: conclusion

- Advantage
  - fast
- Disadvantage
  - not QDI
  - a small area overhead

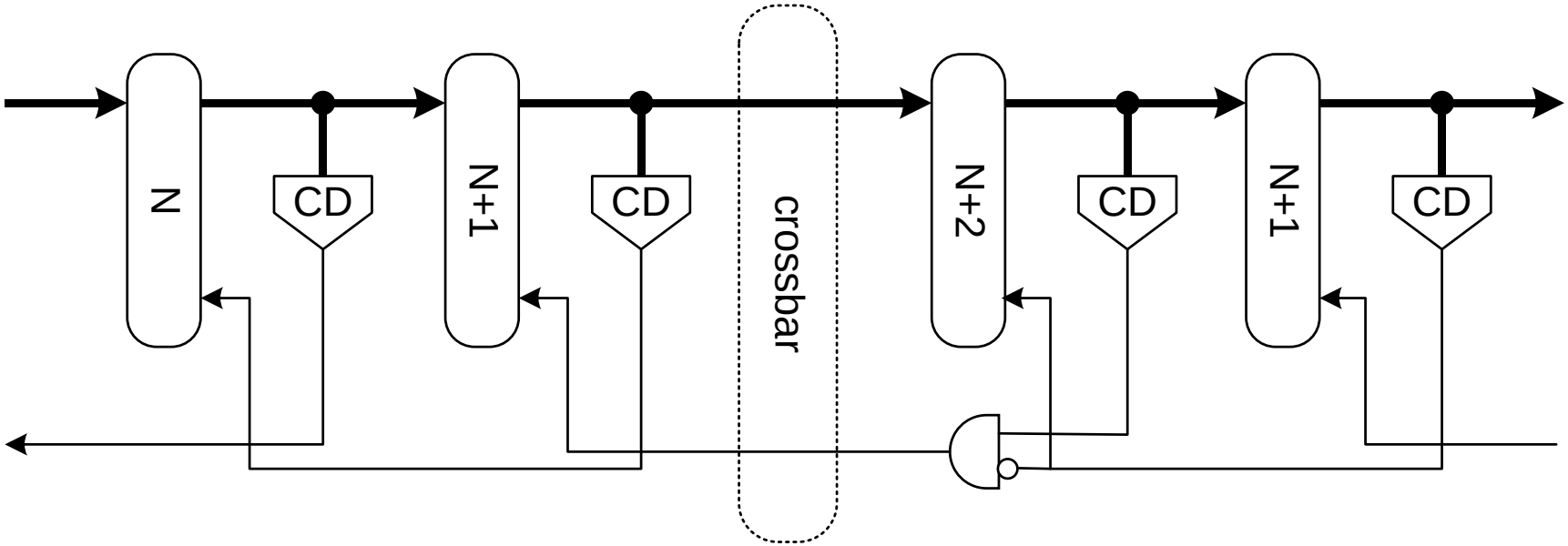




Lookahead: critical cycle



Lookahead: implementation



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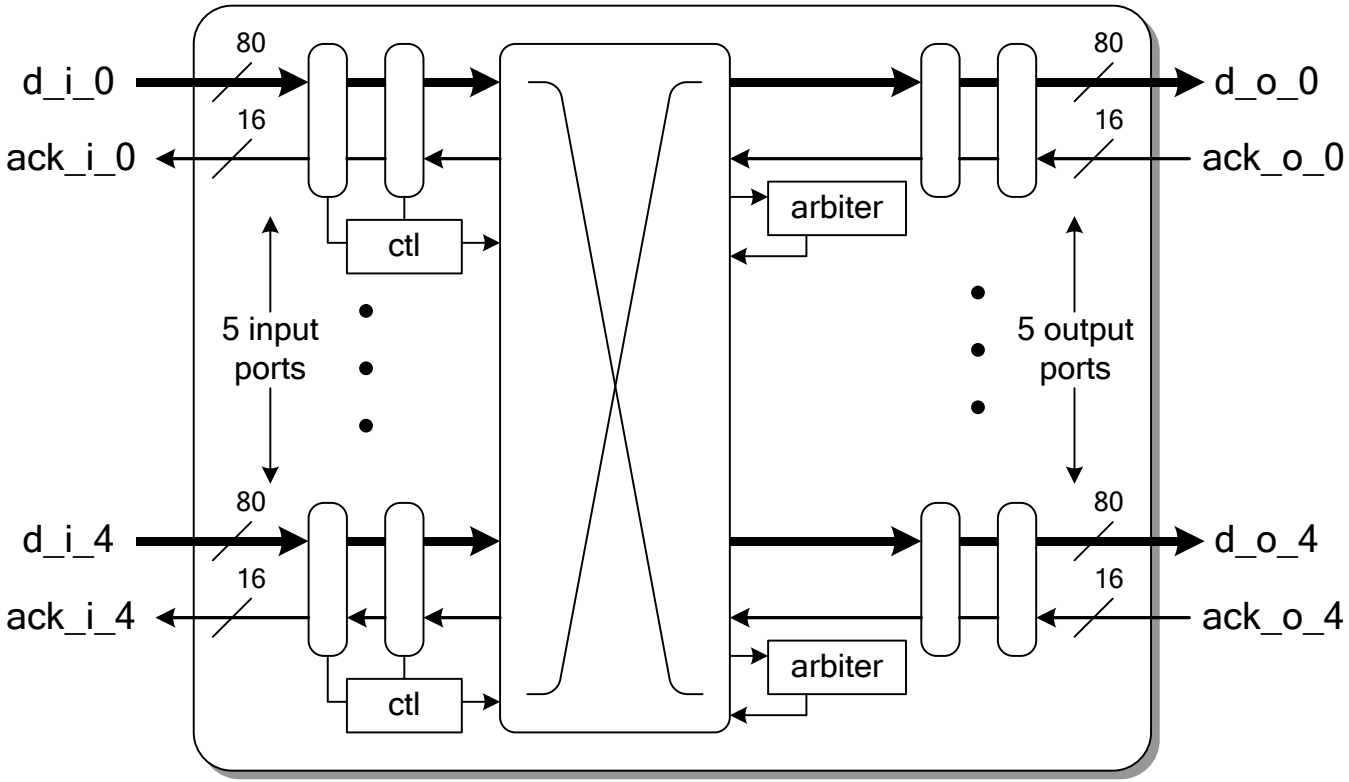
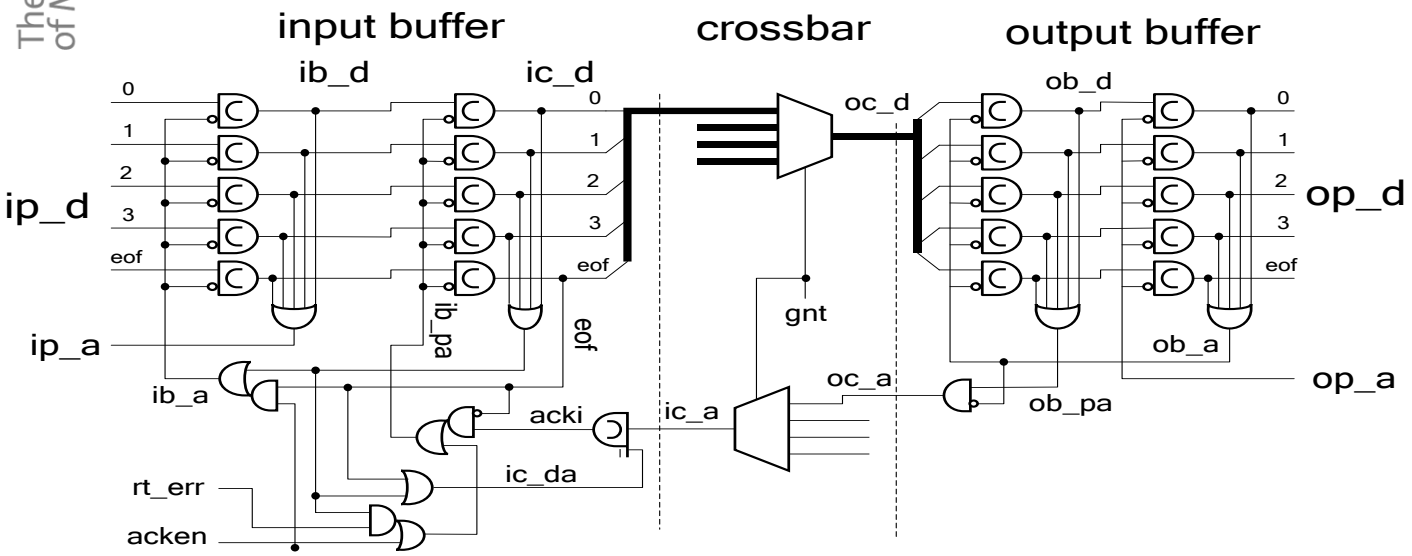
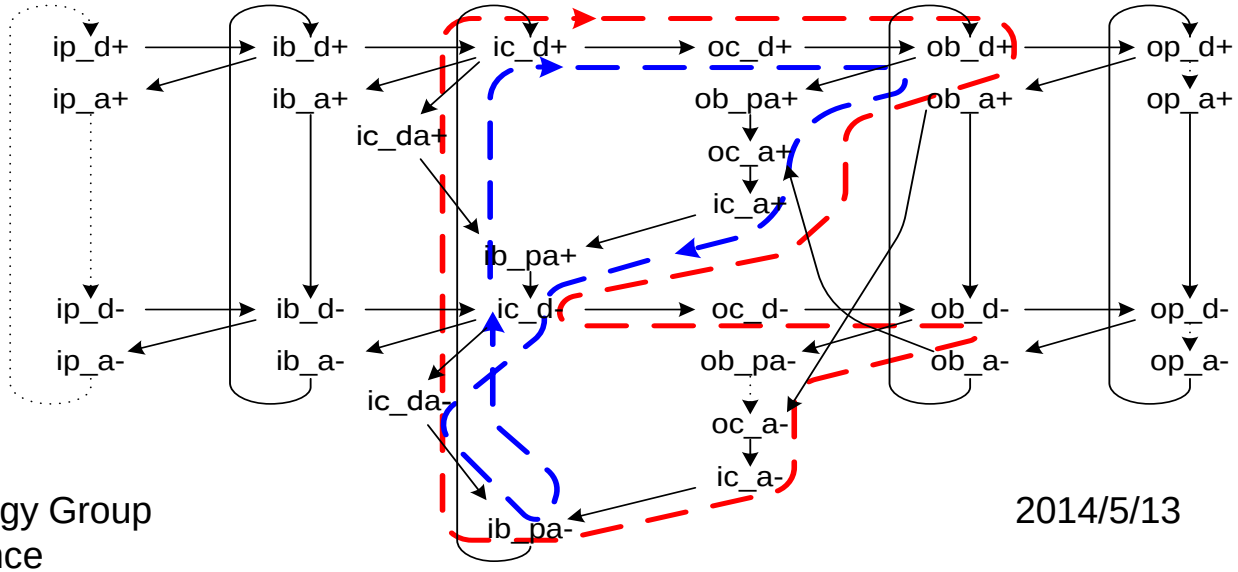
Router: structure



Router: data path





Router: layout

- Faraday 130nm Technology
- 32-bit, 5 ports, XY routing algorithm
- 0.3x0.3mm (14.3K gates, 0.057mm^2)
- Typical corner (25 ^{o}C 1.2V)
- Cycle period 1.7 ns (2.35GByte/s per port)

ChSlice and Lookahead

	ChSlice & LH	ChSlice	No ChSlice/LH
Period	1.7 ns	2.2 ns	2.9 ns
Latency	1.7 ns	2.1 ns	2.8 ns
Route Overhead	0.8 ns	0.8 ns	0.8 ns

Block	ChSlice & LH	ChSlice	No ChSlice/LH
Input Buffers	6.2K	5.8K	4.3K
Output Buffers	4.5K	4.5K	4.4K
Crossbar	3.3K	3.2K	2.4K
Other	0.5K	0.4K	0.2K
Total	14.5K	13.9K	11.3K

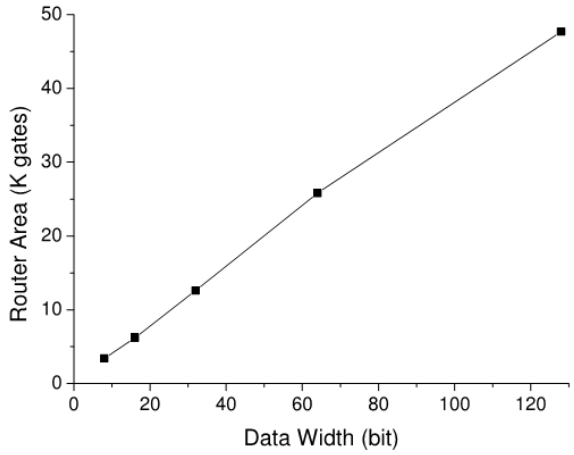
Speed: ChSlice 24.1% LH 17.2% Area: ChSlice 23.0% LH 5.3%

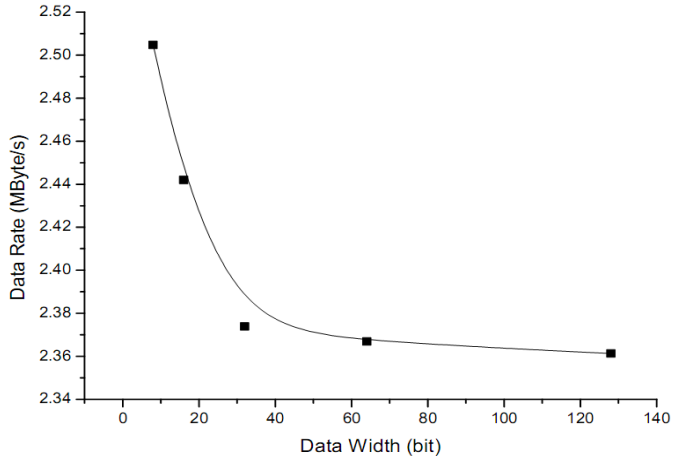
Compare to other routers

- MANGO: 1.26ns; 0.12um; bundled data
- ANoC: 4ns; 0.13um; 1-of-4
- QNoC: 4.8ns; 0.18um; bundled data
- ASPIN: 0.88ns; 90nm; dual-rail & bundled data
- Our: 1.7ns; 0.13um; 1-of-4 & lookahead

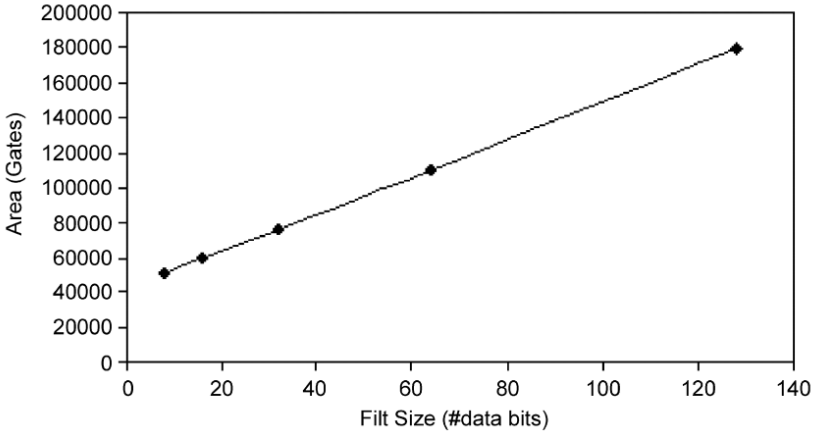
Speed vs. data width

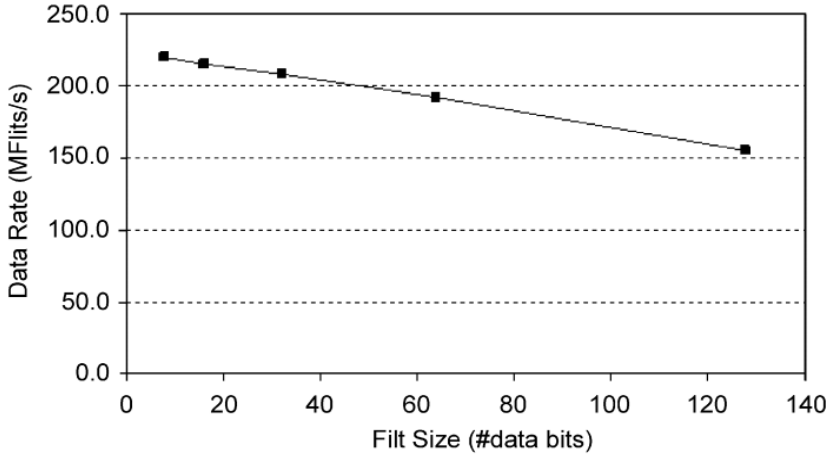
Wormhole





QNoC





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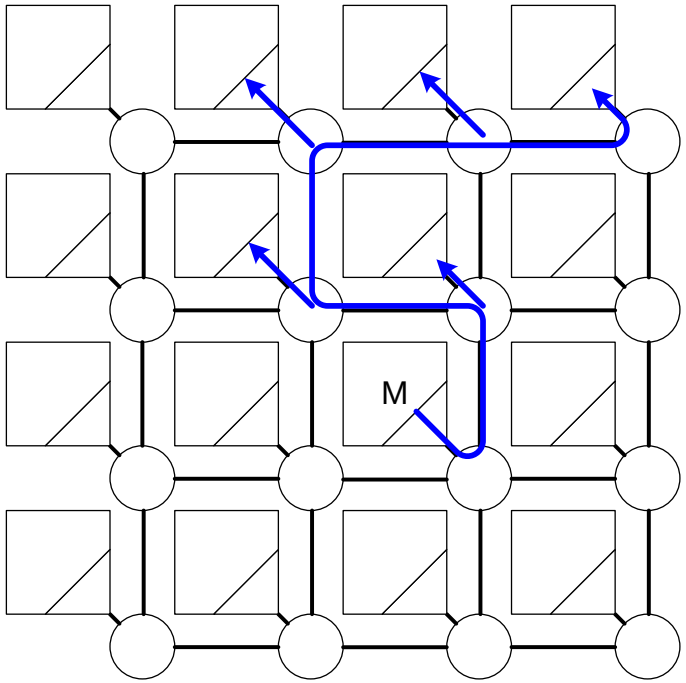
XY/Stochastic

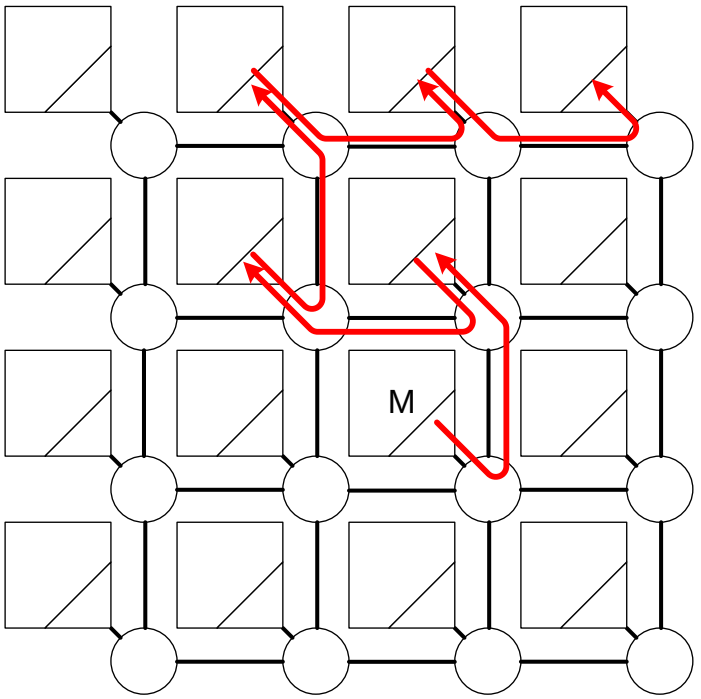
- Motive
  - Two routing algorithm is complicated
  - The deadlock problem
  - The involvement of network interfaces
  - Keep router simple
- Solution
  - Router: XY
  - Network interface: generate, consume, or forward (random)

XY/Stochastic (request path)

Router Only

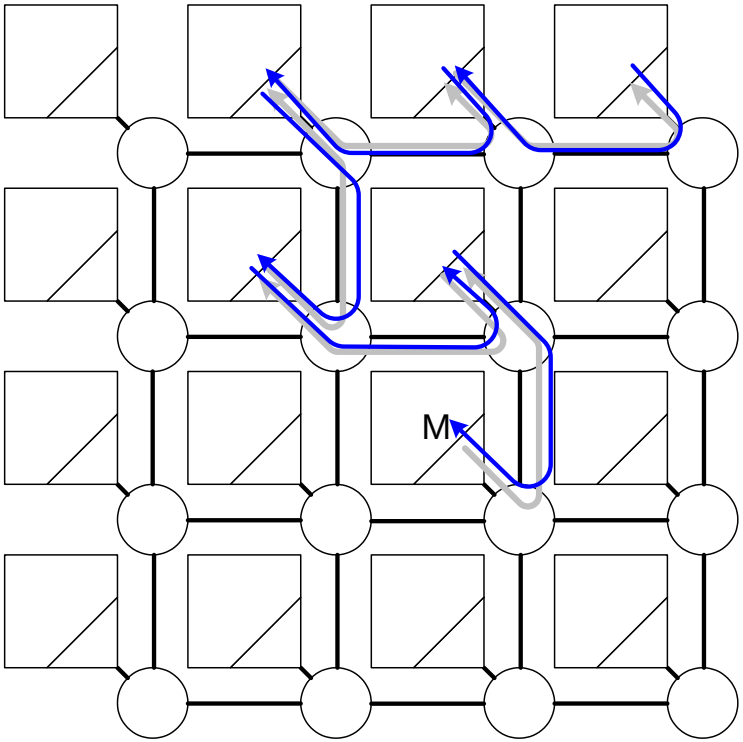


XY/Stochastic

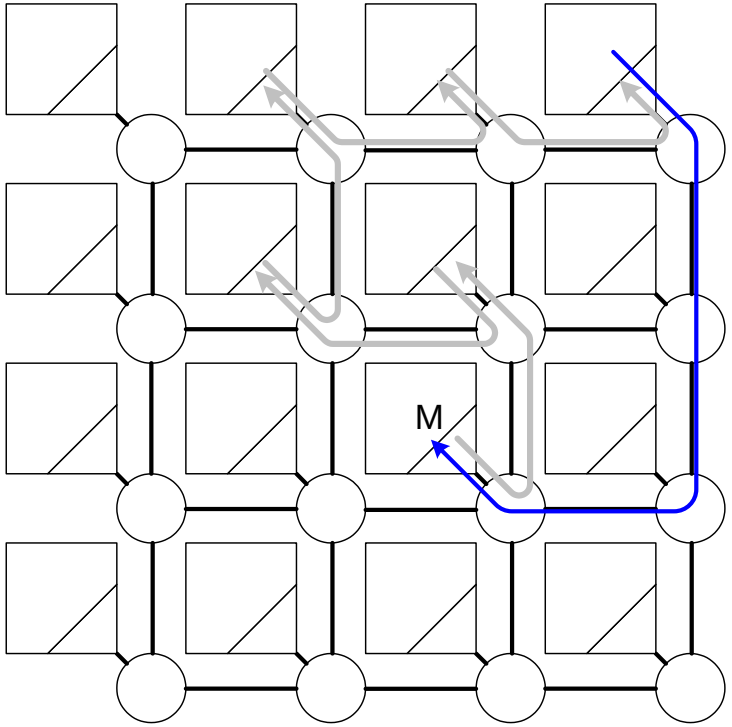


XY/Stochastic (ack path)

Same Path



Single Jump



Compare

- Rely on routers
  - A larger router (Special router design)
  - Longer routing overhead
  - Deadlocks
  - Shorter search time
- XY/Stochastic routing
  - Smaller router (normal router design)
  - Shorter routing time
  - Only deadlocks caused by errors
  - Longer search time (higher priority by QoS)

Conclusion

- Router design plan
  - Wormhole router is the first step
- Wormhole router
  - Channel slicing
  - SDM is better than TDMA for asynchronous routers
- XY/Stochastic routing

Question?