

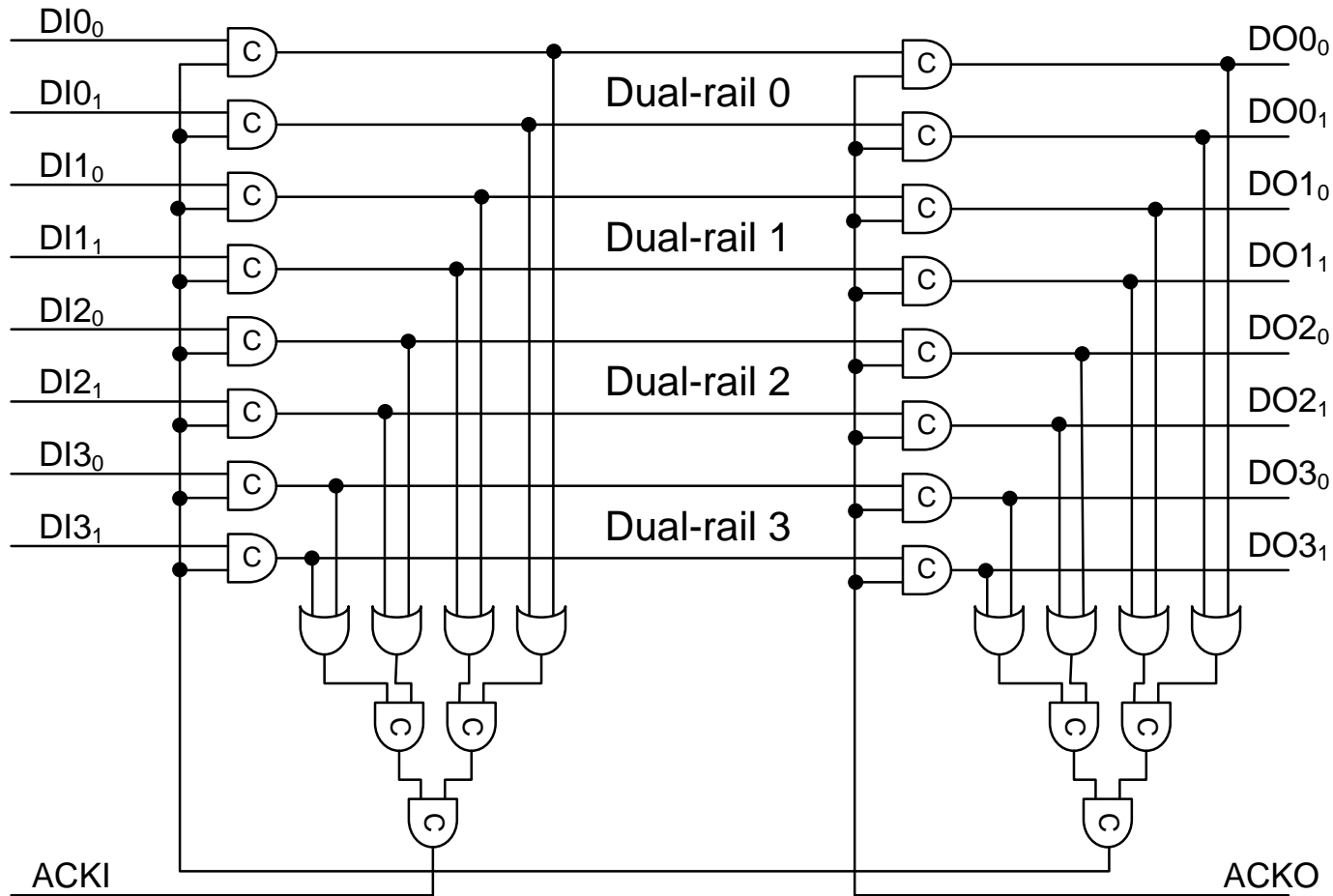
The Simulation of the Dynamic Link Allocation Router (DyLAR)

Wei Song

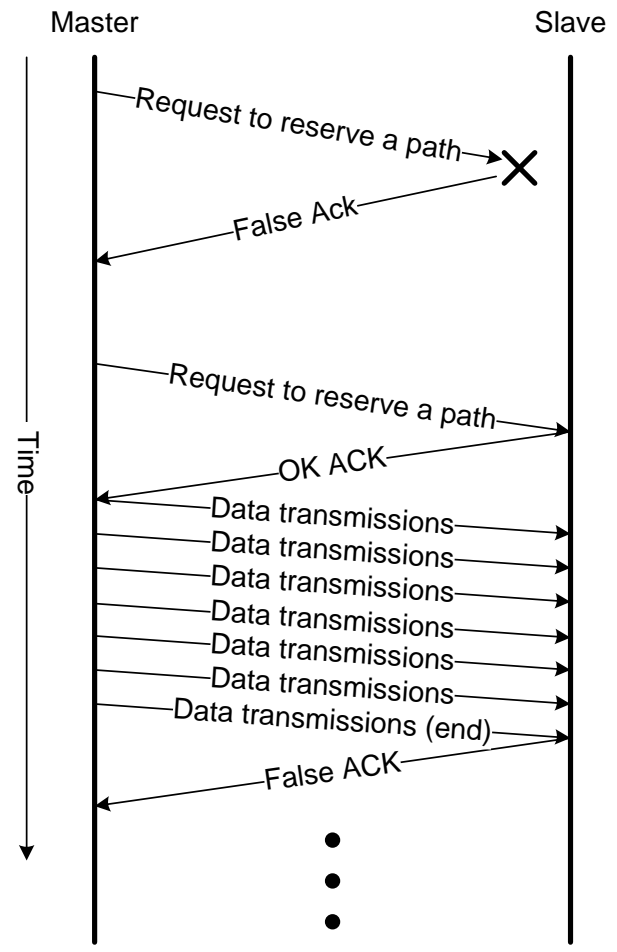
Overview

- A brief review of the *Dynamic Link Allocation* flow control method
- The new simulation platform
- Some simple performance analyses
- An alternative method of the *task request procedure*
- Future schedule

Serial is better than Parallel

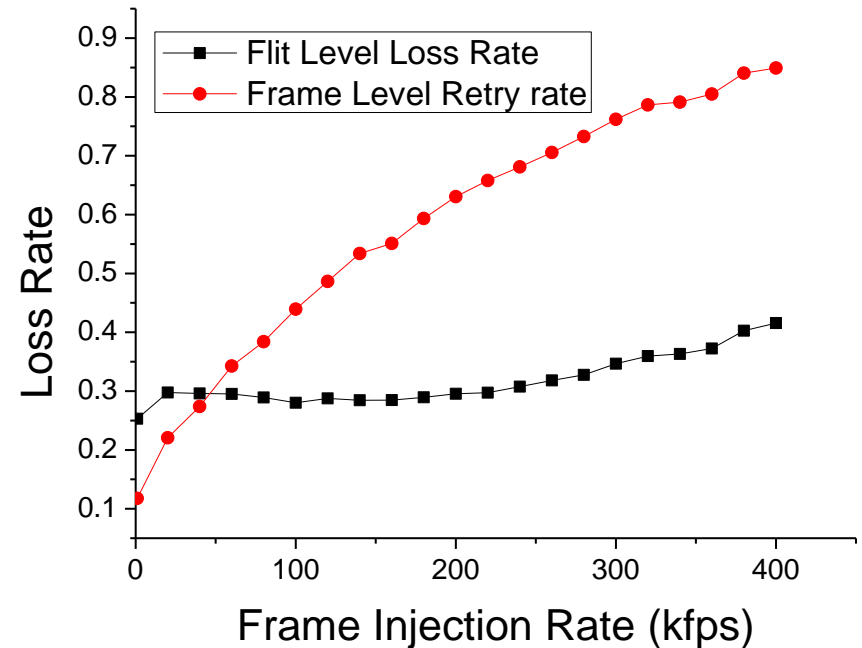
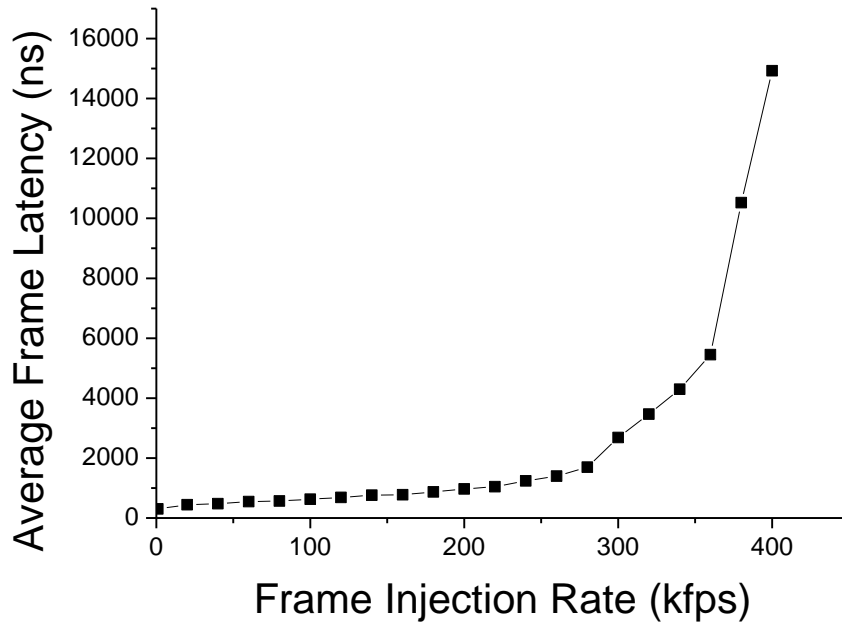


Bandwidth efficiency is less than 50%



The high Loss Rate

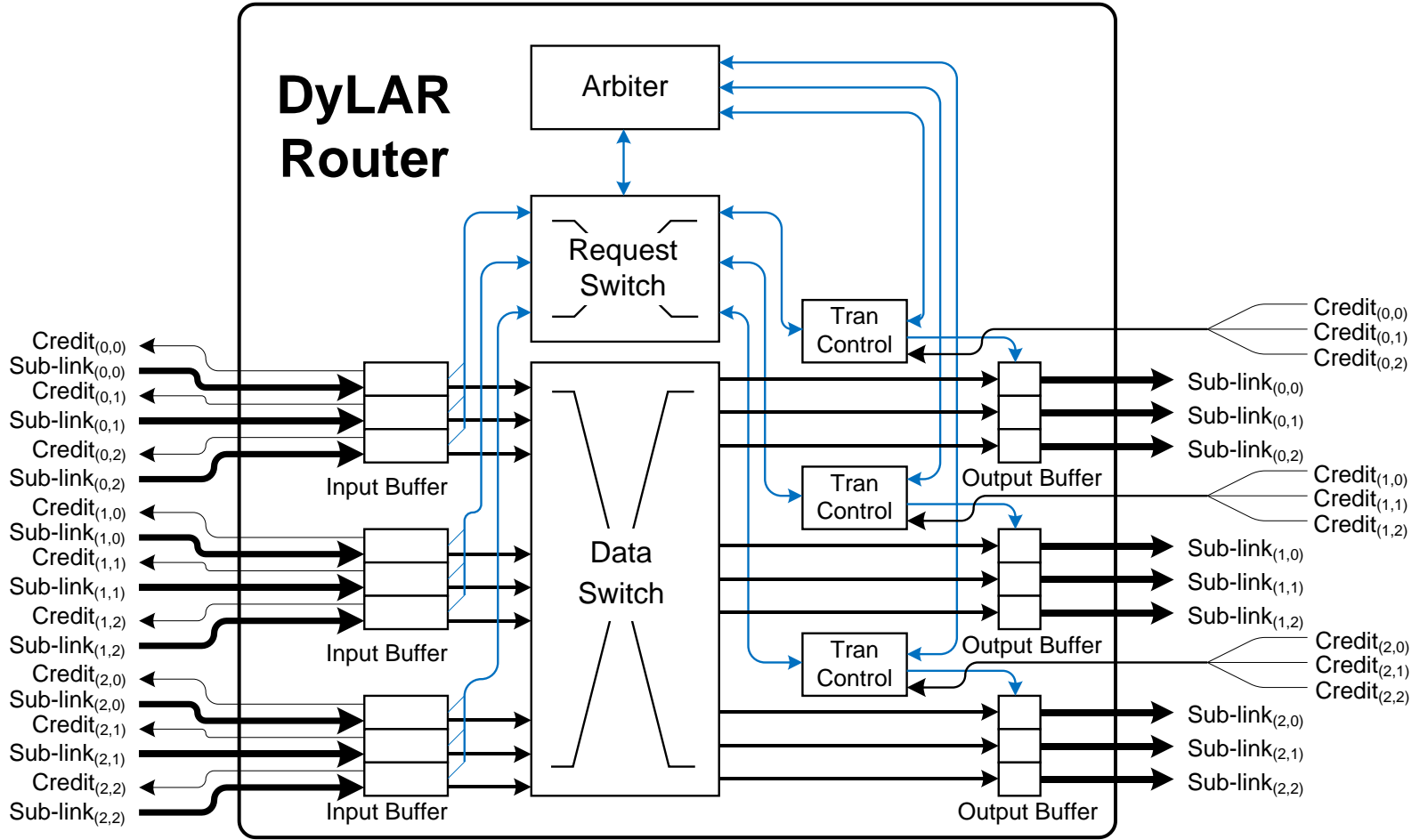
Simulation results of a 6x6 NoC.



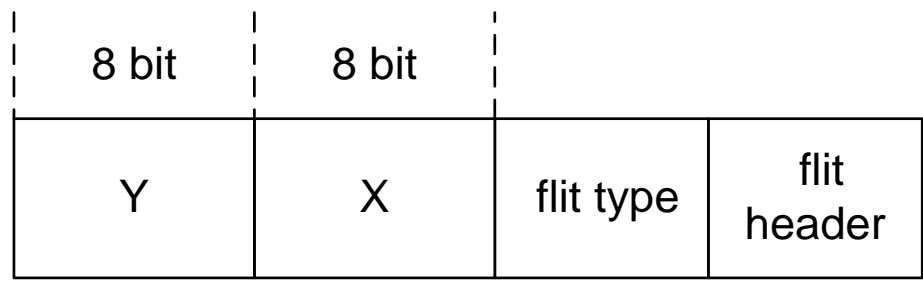
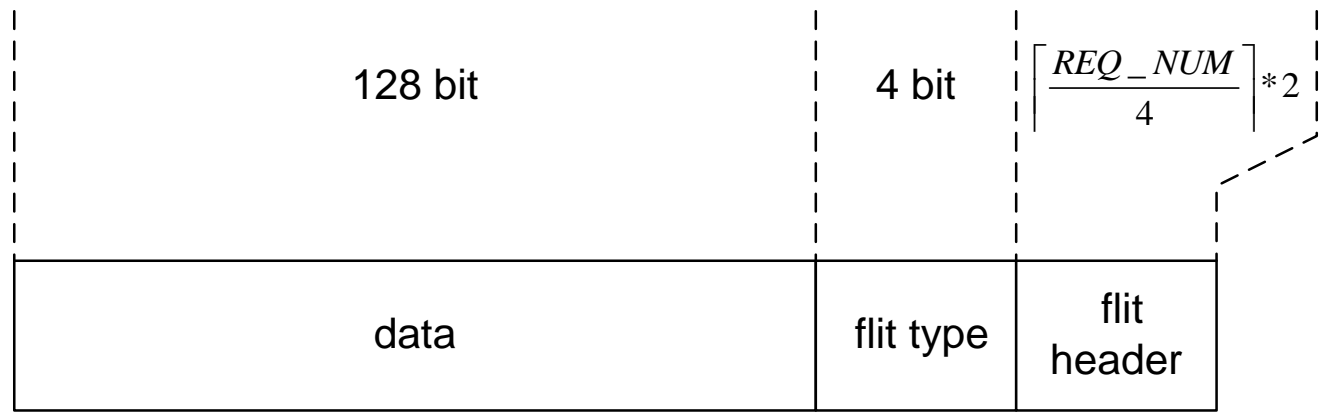
Some hypotheses of *DyLAR*

- Asynchronous circuits prefer serial rather than parallel channels
- Connection oriented communications only have a bandwidth efficiency less than 50%
- The high retry rate of connection oriented communication is reducible by add virtual channels
- The input buffer could be smaller than flit size when using serial channels

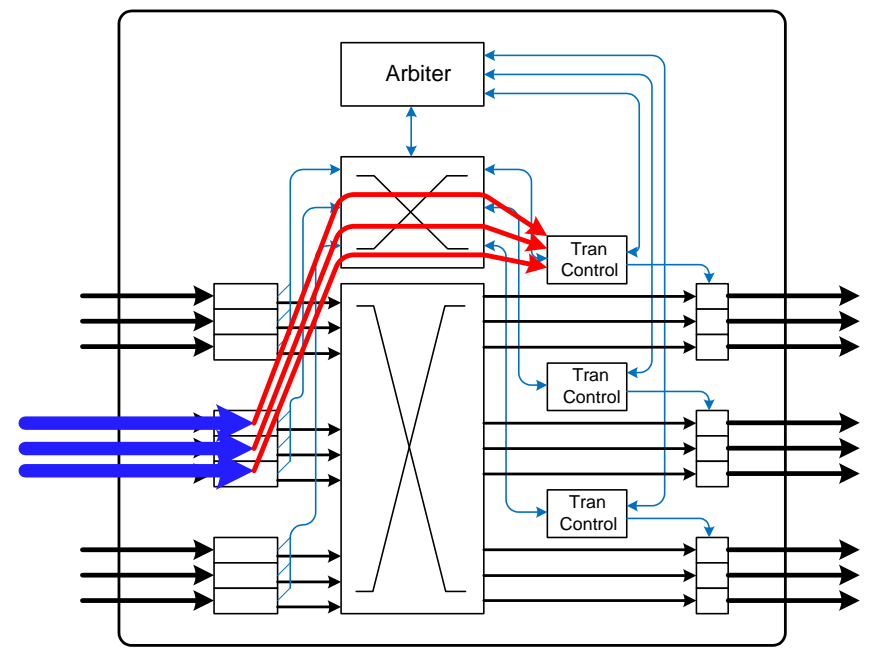
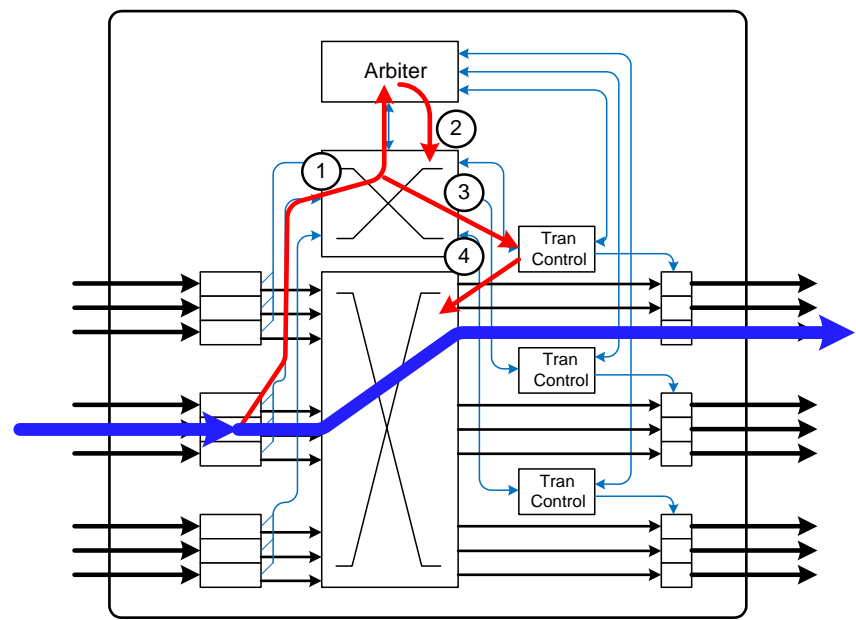
The DyLAR Router



Flit Formats



The Flow Control Procedures



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Basic information

- Mesh topology
- Only send XY frames
- Parameter reconfigurable
- Latency is set according to 1-of-4 CHAIN link
- SystemC 2.2.0
- GNU g++
- Makefile
- Batch simulation and automatic result analysis (accepted traffic, latency, loss rate)

Configurable parameters

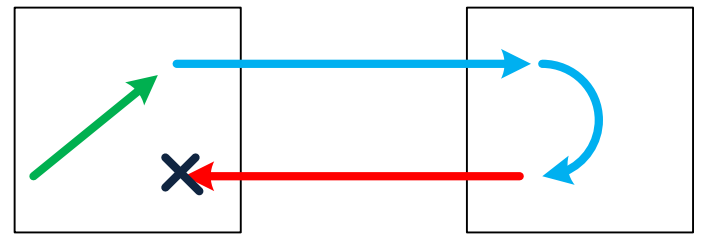
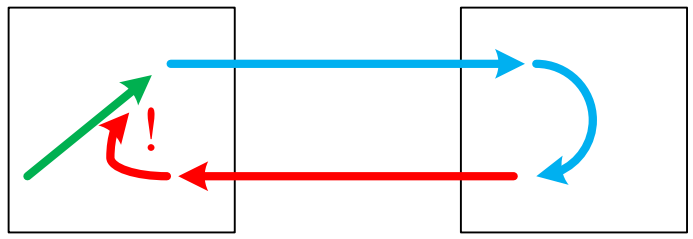
- Dimension (>1)
- Injected traffic (kfps) (>0)
- Channel number (>0)
- Request number (>0)
- Random seed (0 random seed, others seeds)
- Random delay
- Simulation time
- VCD file (generate waveform and debug logs)

Current Problems

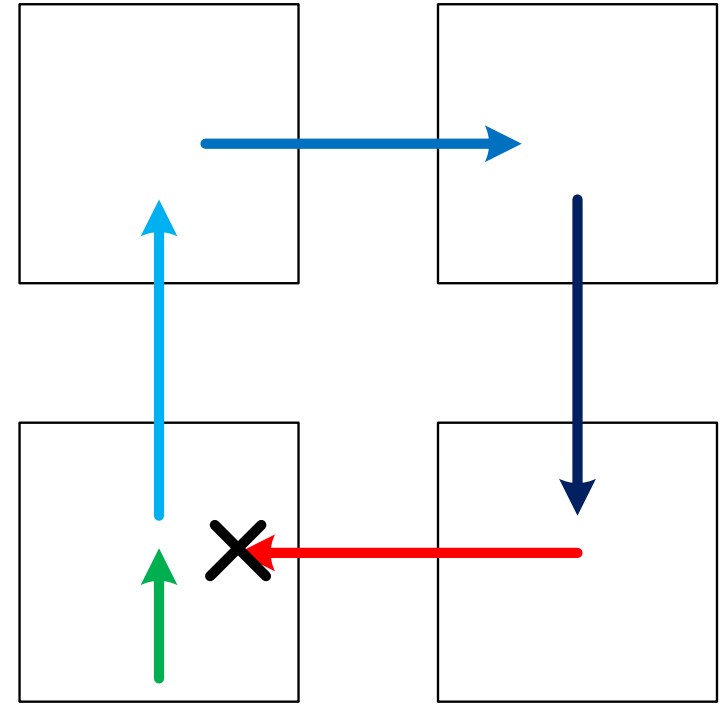
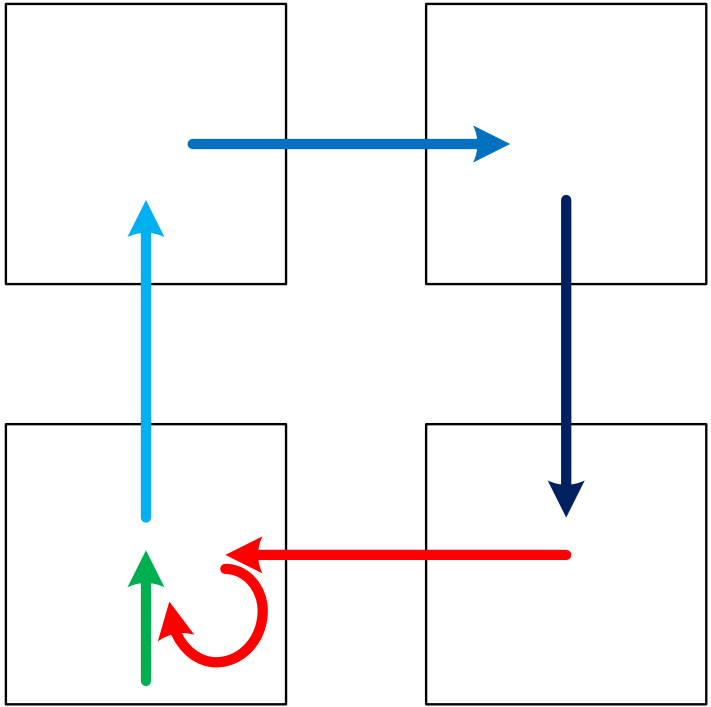
- The router design
 - Multiple request lines sharing one channel will generate deadlocks
 - (still under debugging and modifying)
- The simulation model
 - Slow (possible > 20 min under 4x4 cases)
 - Memory consuming (possible $> 2G$ under some 4x4 cases)

Simulation environment: ADM 2.4GHz 64-bit 4G memory

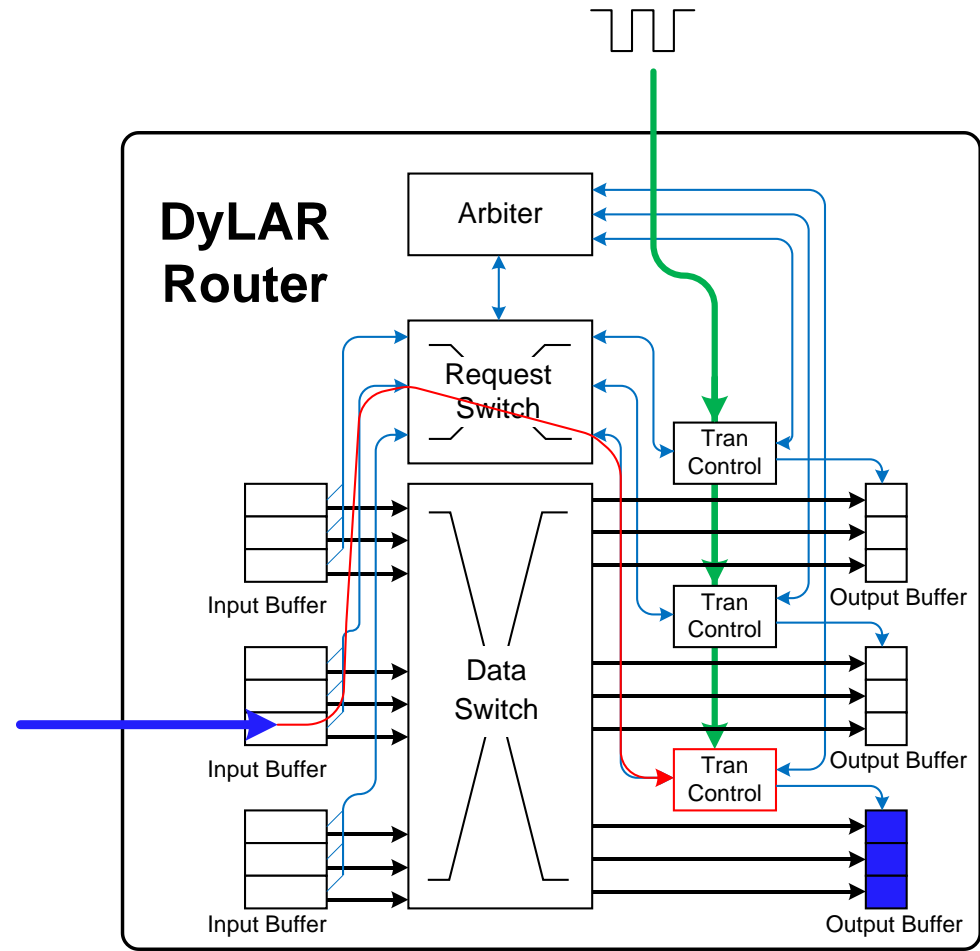
Deadlock Avoidance 1



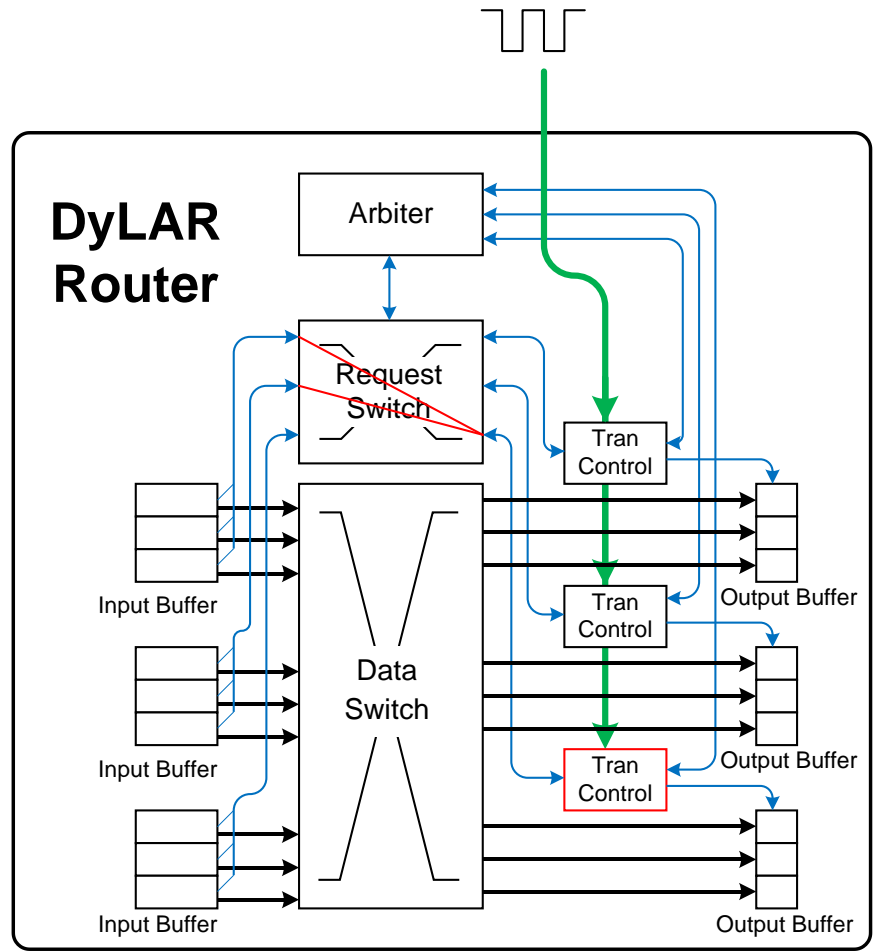
Deadlock Avoidance 2



Deadlock Recovery 1



Deadlock Recovery 2



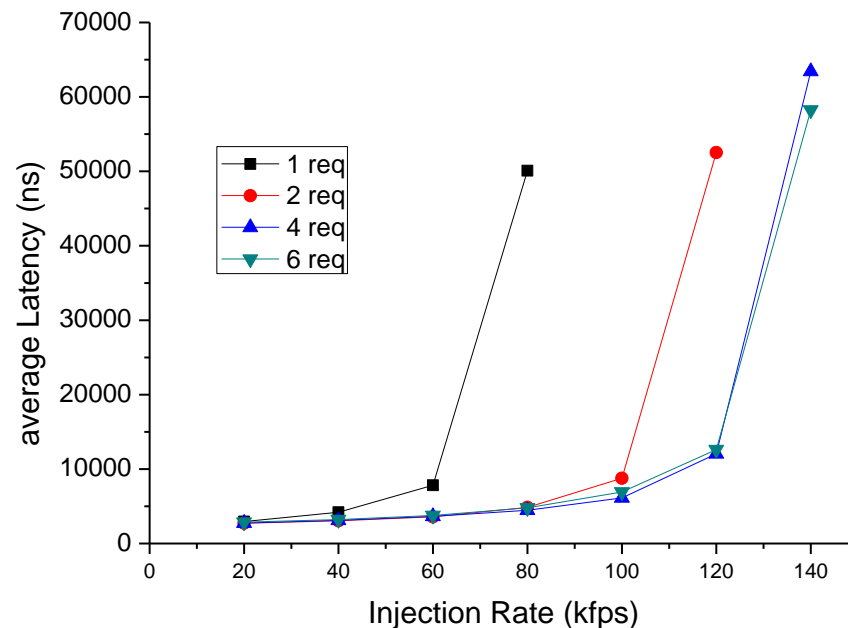
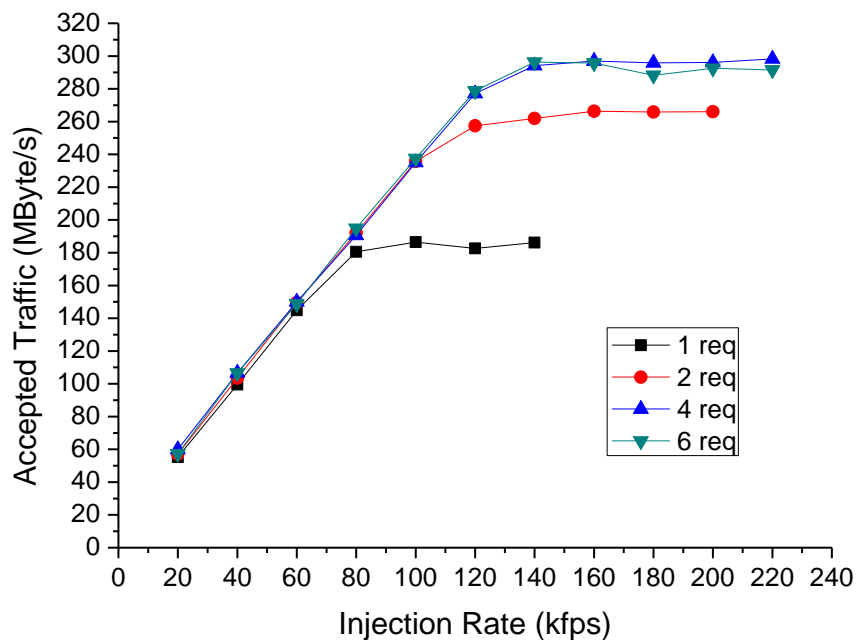
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- **Some simple performance analyses**
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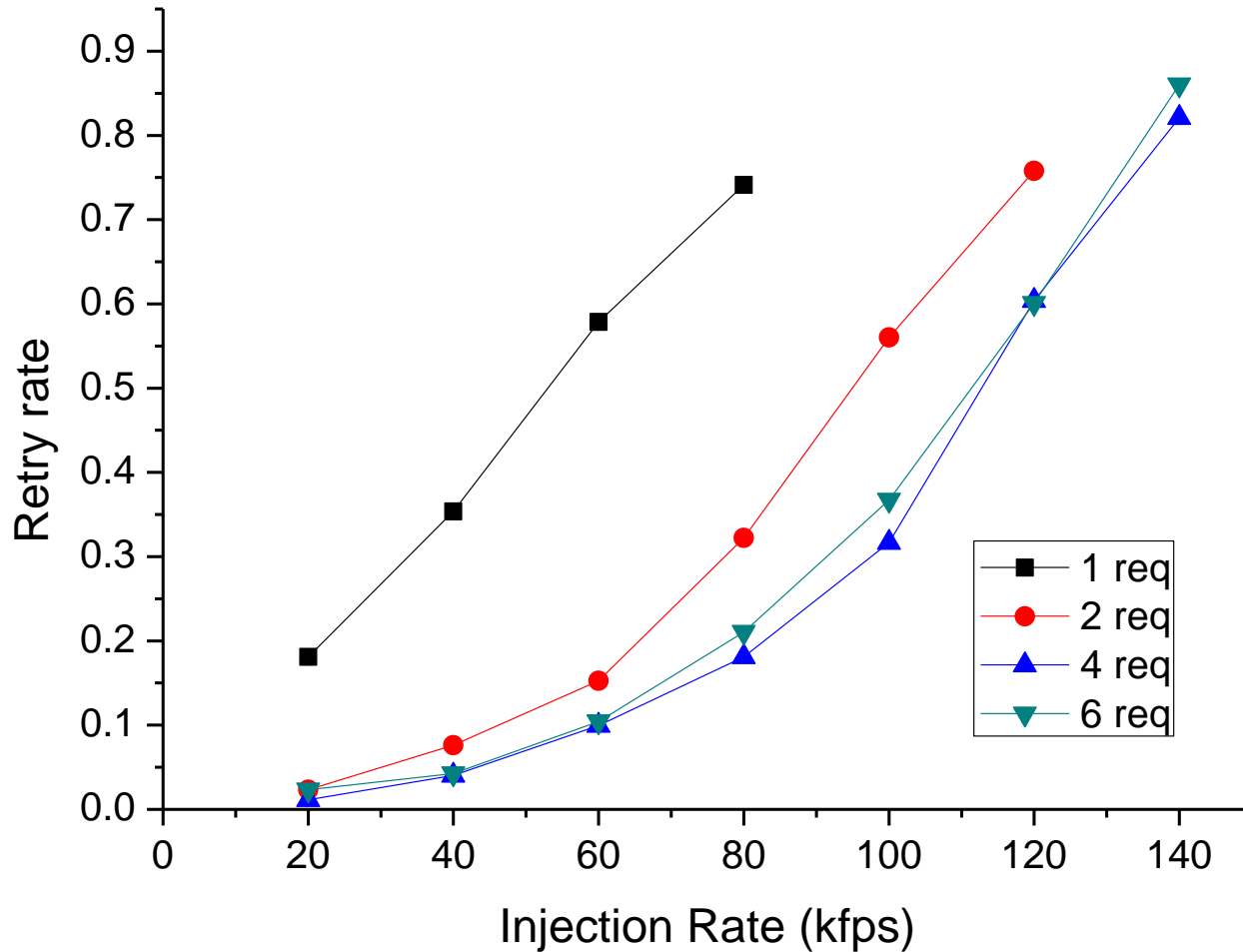
Simulation parameters

- Dimension 4x4
- Channel 1~3
- Request line 1~8
- Frame injection rate 20~500 kfps
- Random delay and random uniform traffic pattern

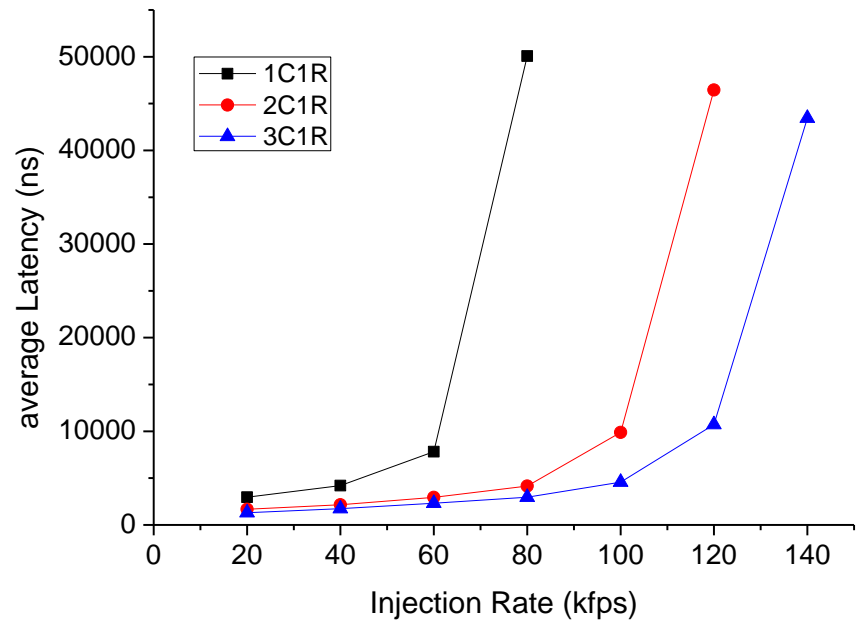
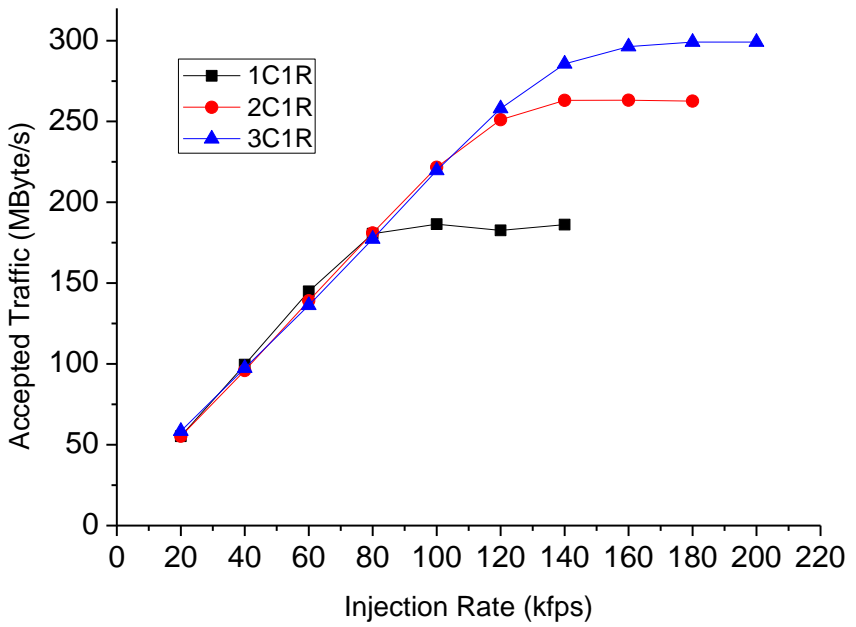
1 channel with multiple requests



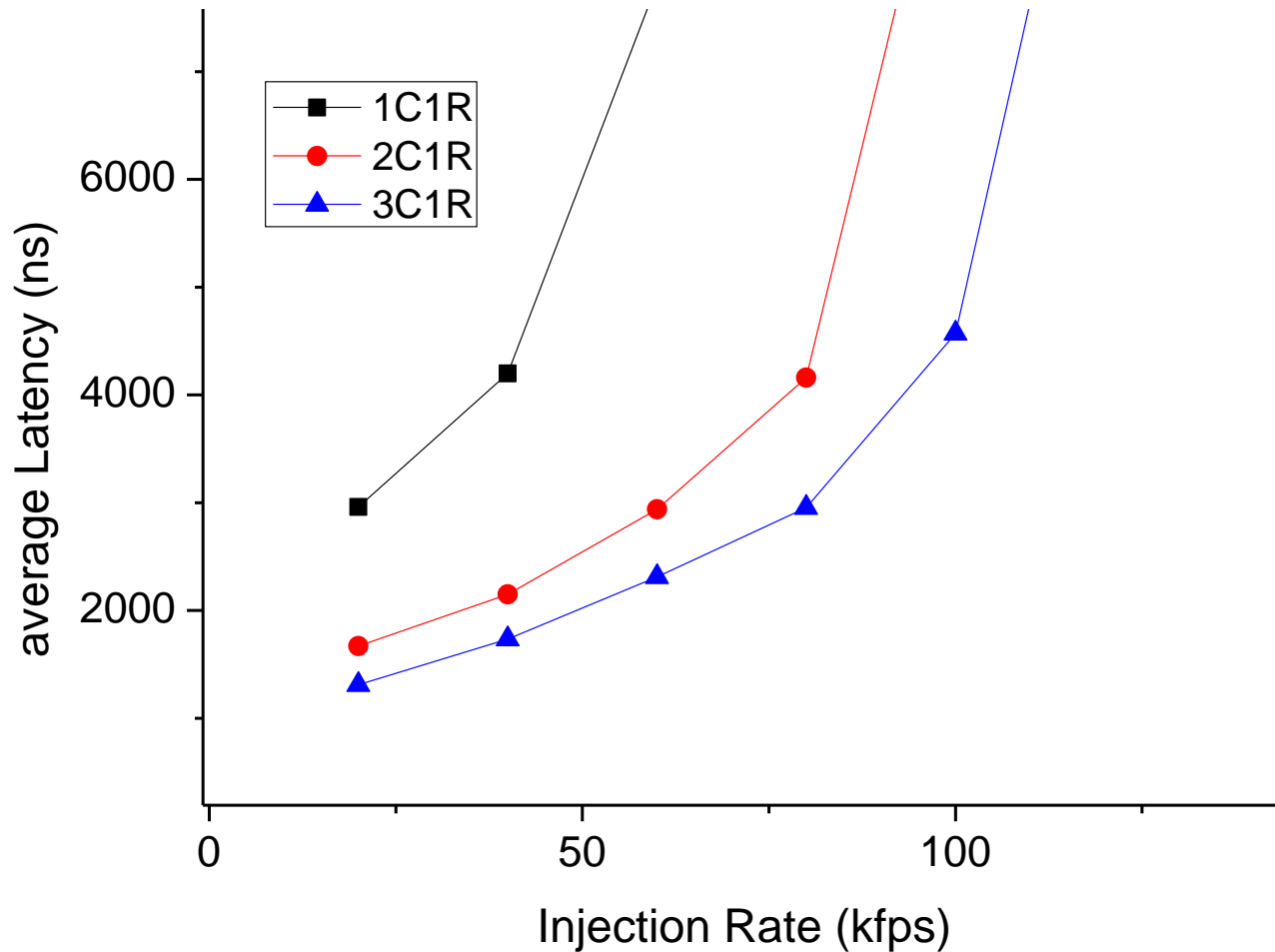
1 channel with multiple requests



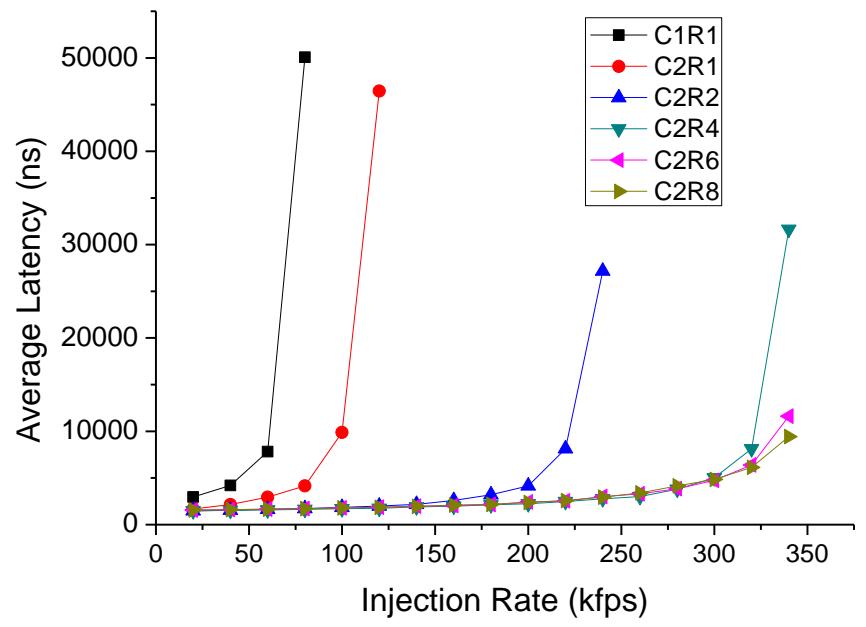
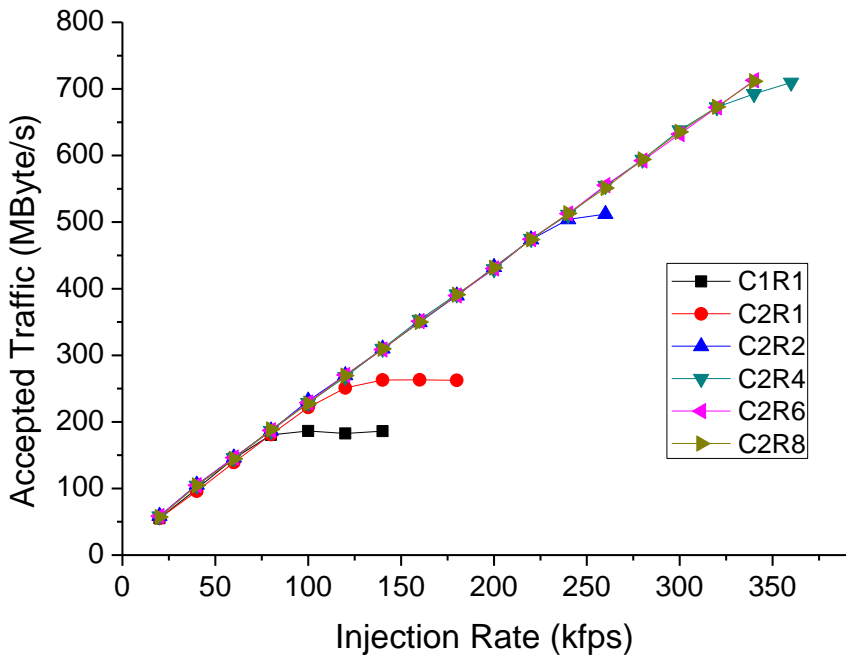
1 request with multiple channels



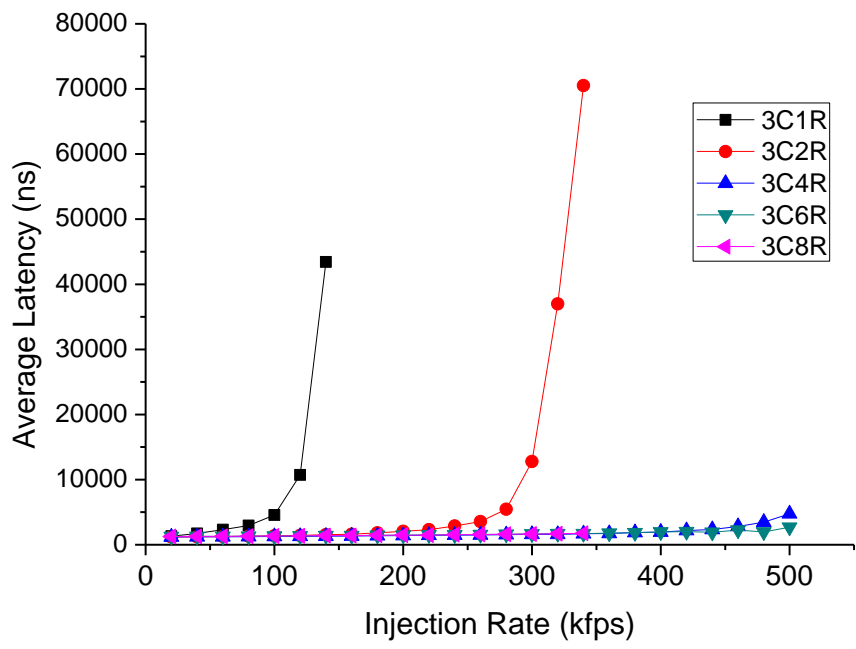
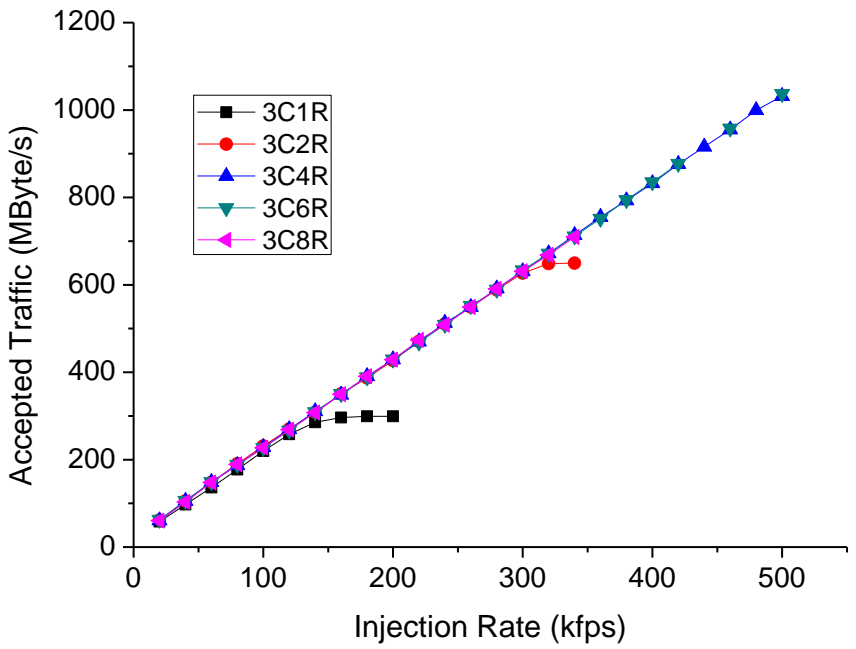
1 request with multiple channels



2 channels with multi-requests



3 channels with multi-requests



Throughput

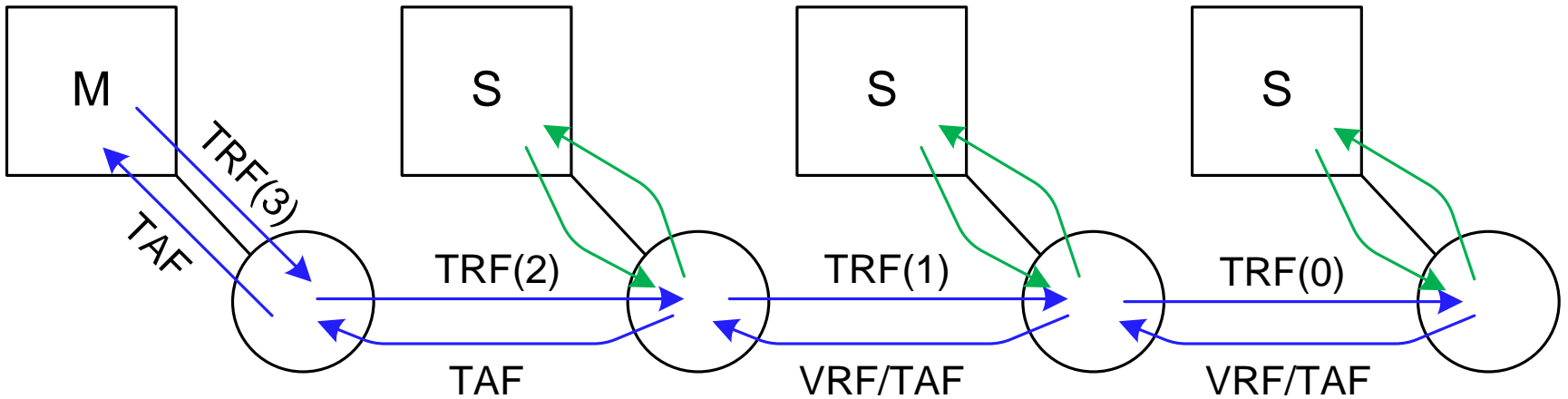
	1 request	2 request	4 request	6 request	8 request
1 channel	186	266	300	300	300
2 channel	265	512	710	>710	>710
3 channel	300	650	>1000	>1000	>1000

Unit: MByte/s

Overview

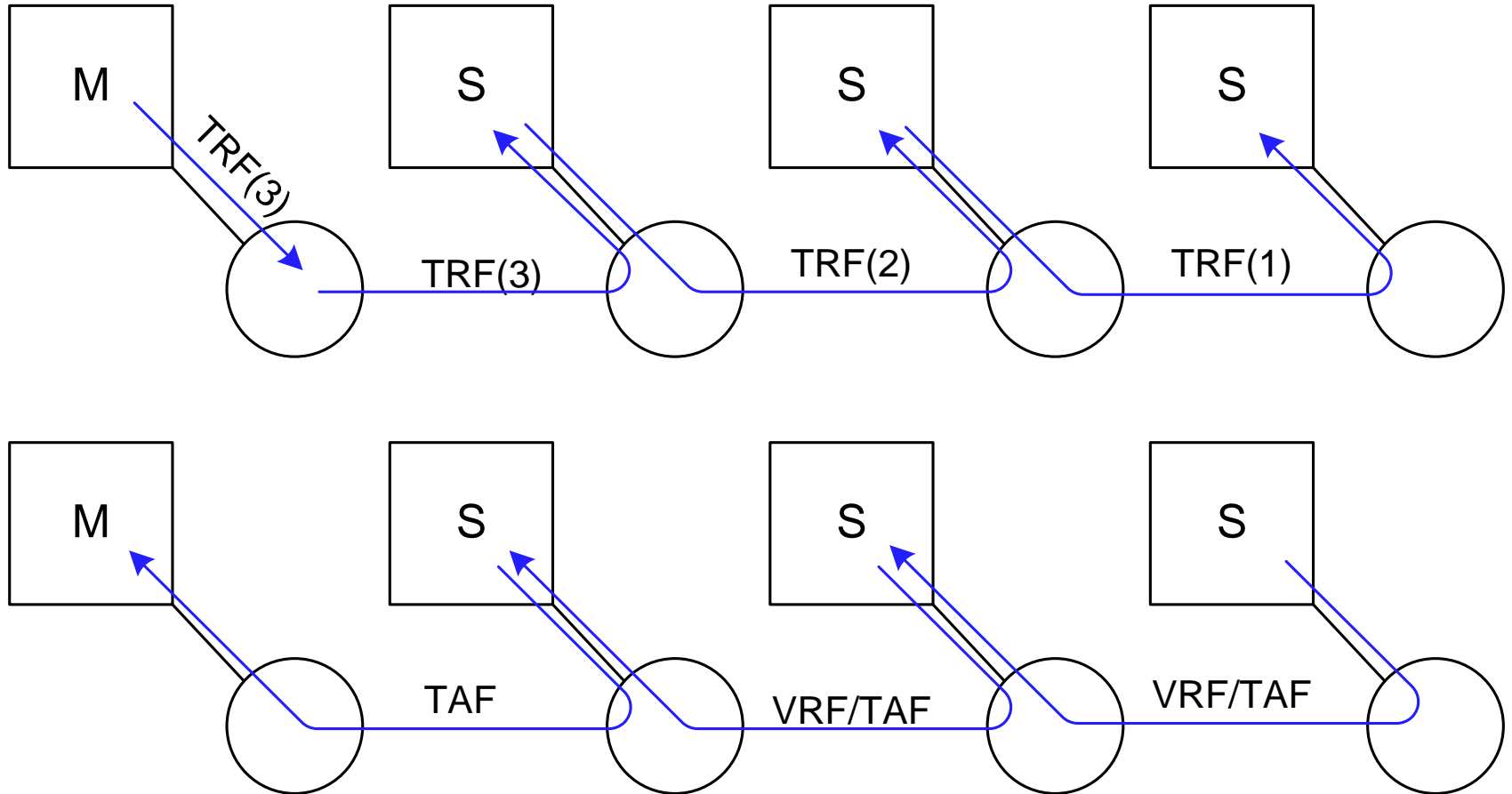
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The Original Task Request Procedure



TRF task request flit
VRF volunteer request flit
TAF task acknowledge flit

The alternative method



Comparison of the two methods

- The original TRF
 - Need counters to calculate `life_time`
 - Remember state for every TRF
 - Special communication with NA
 - Wait for the whole flit
 - One request line per TRF
- The alternative
 - Move counters to NA
 - States will be recorded by NA and only 1 state machine is enough
 - Directly send flit to NA
 - Send directly after the `flit_type` field
 - Two request lines per TRF

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Schedule

- The simulation model is still under debugging
- Build the hardware model according to the SystemC model
- Try to speed up the simulation model and reduce the memory required

Thank you!

Questions?