Untethering the Rocket-Chip

Producing a stand-alone lowRISC SoC

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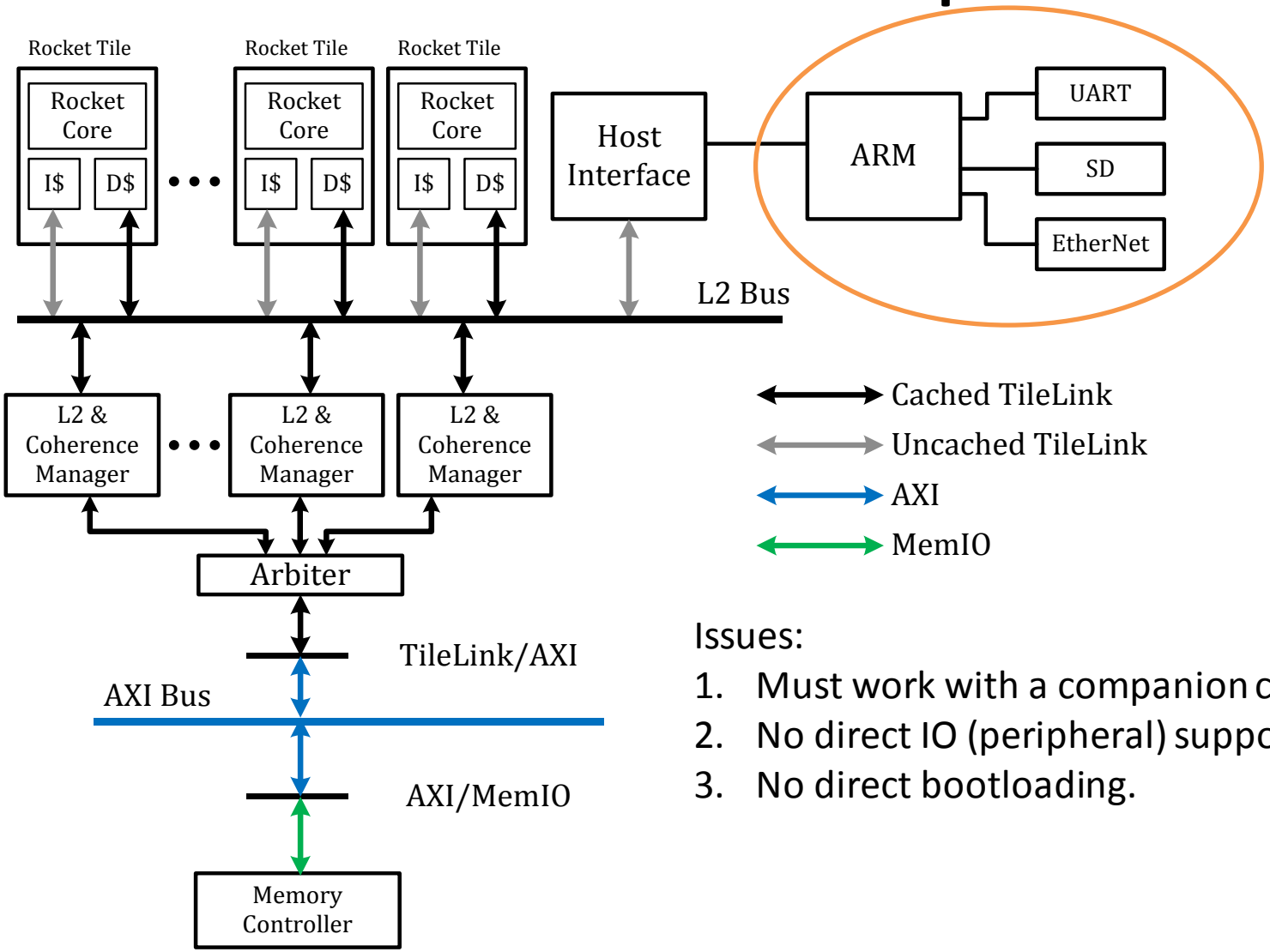
07/10/2015

Background

- Rocket-chip
  - An open-source SoC from UC Berkeley
  - Rocket core
    - RISC-V 64 ISA
    - 5/6 stage single-issue in-order processor
    - Non-blocking L1 D$
    - Performance comparable to ARM Cortex-A5
    - Chisel (RTL, OO, functional)
    - Zynq FPGA (ARM A9), Linux bootable
    - Full cross-compilation tool chain

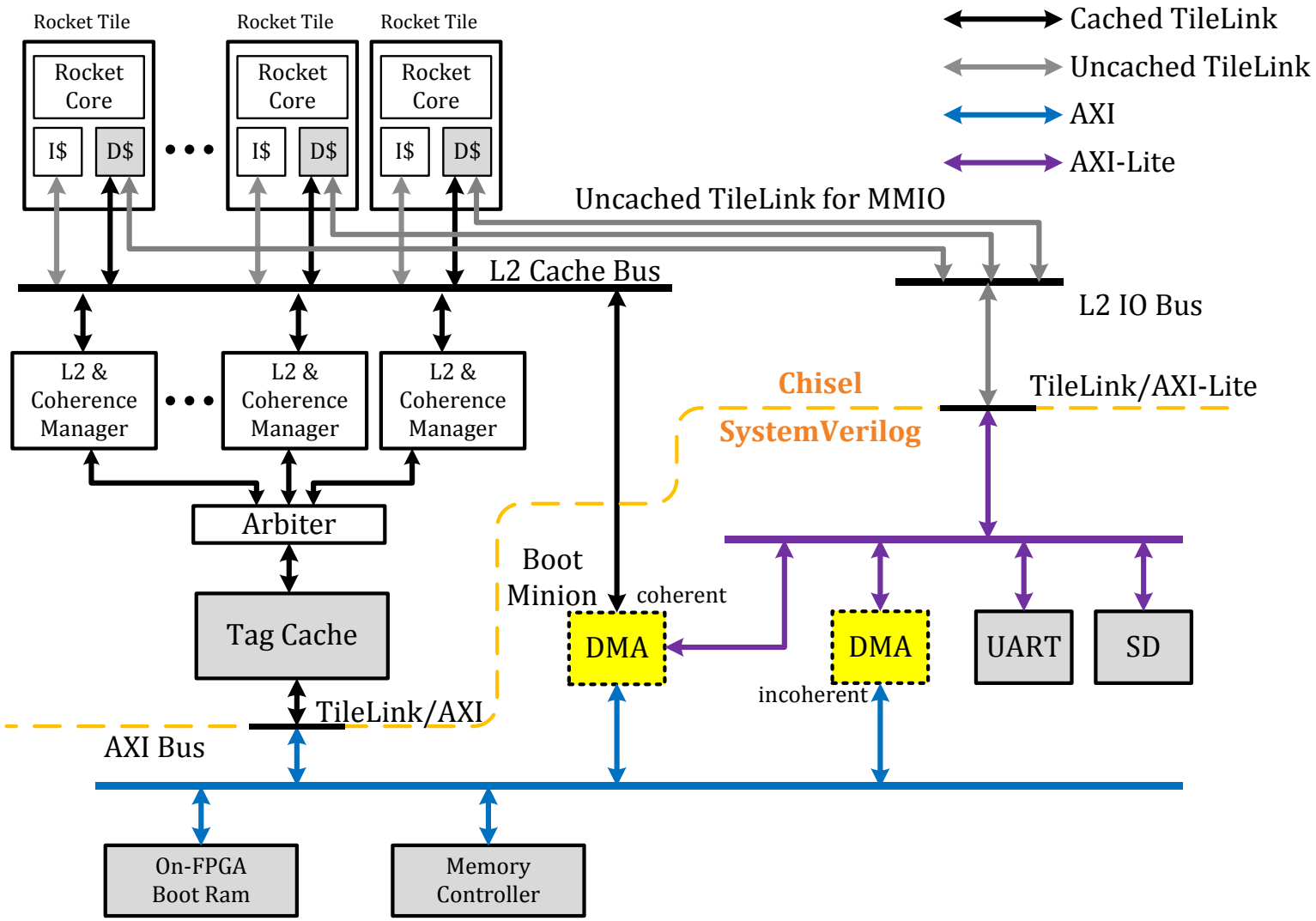
Rocket-Chip



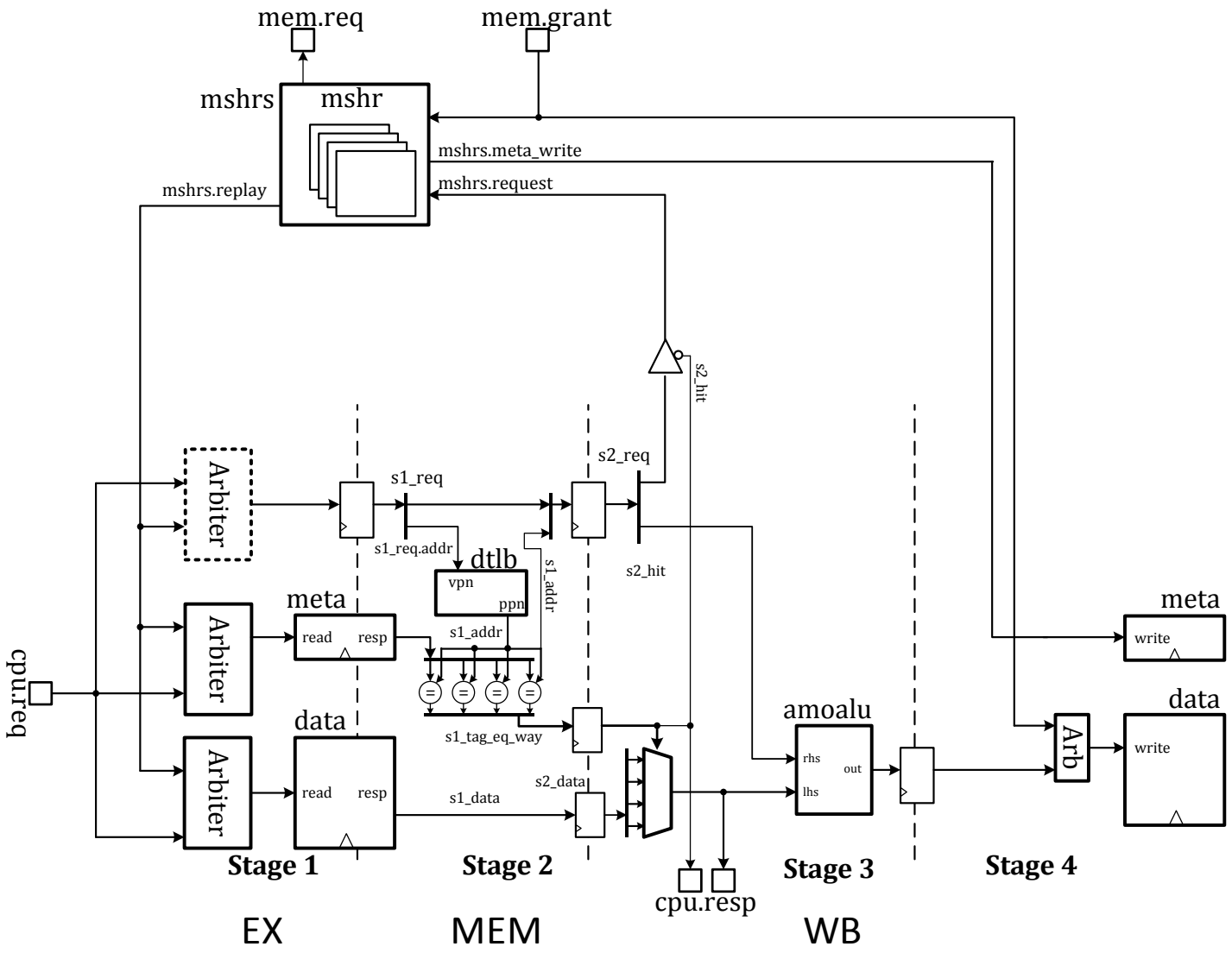
Issues:

1. Must work with a companion core (ARM).
2. No direct IO (peripheral) support.
3. No direct bootloading.

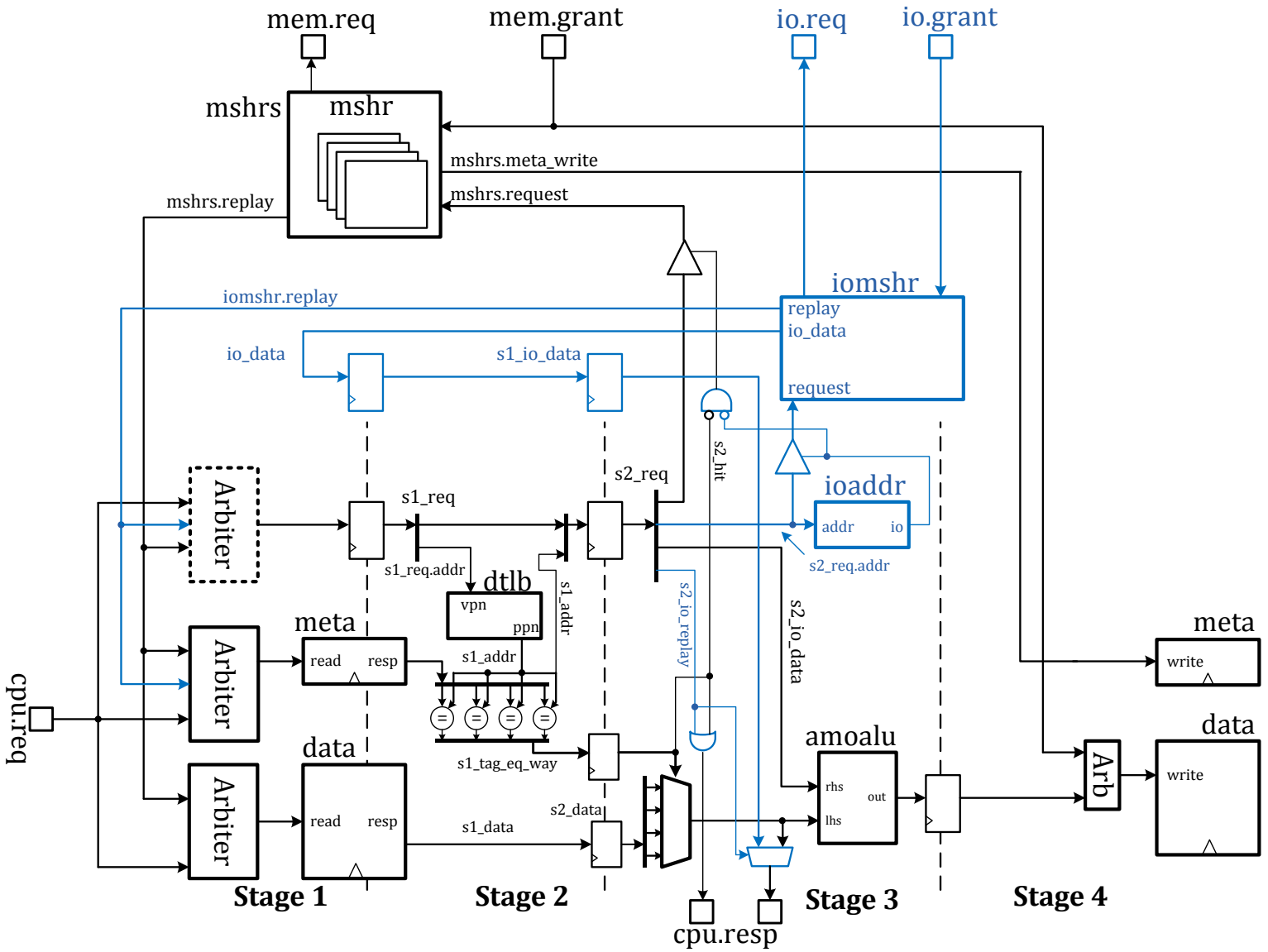
lowRISC-Chip



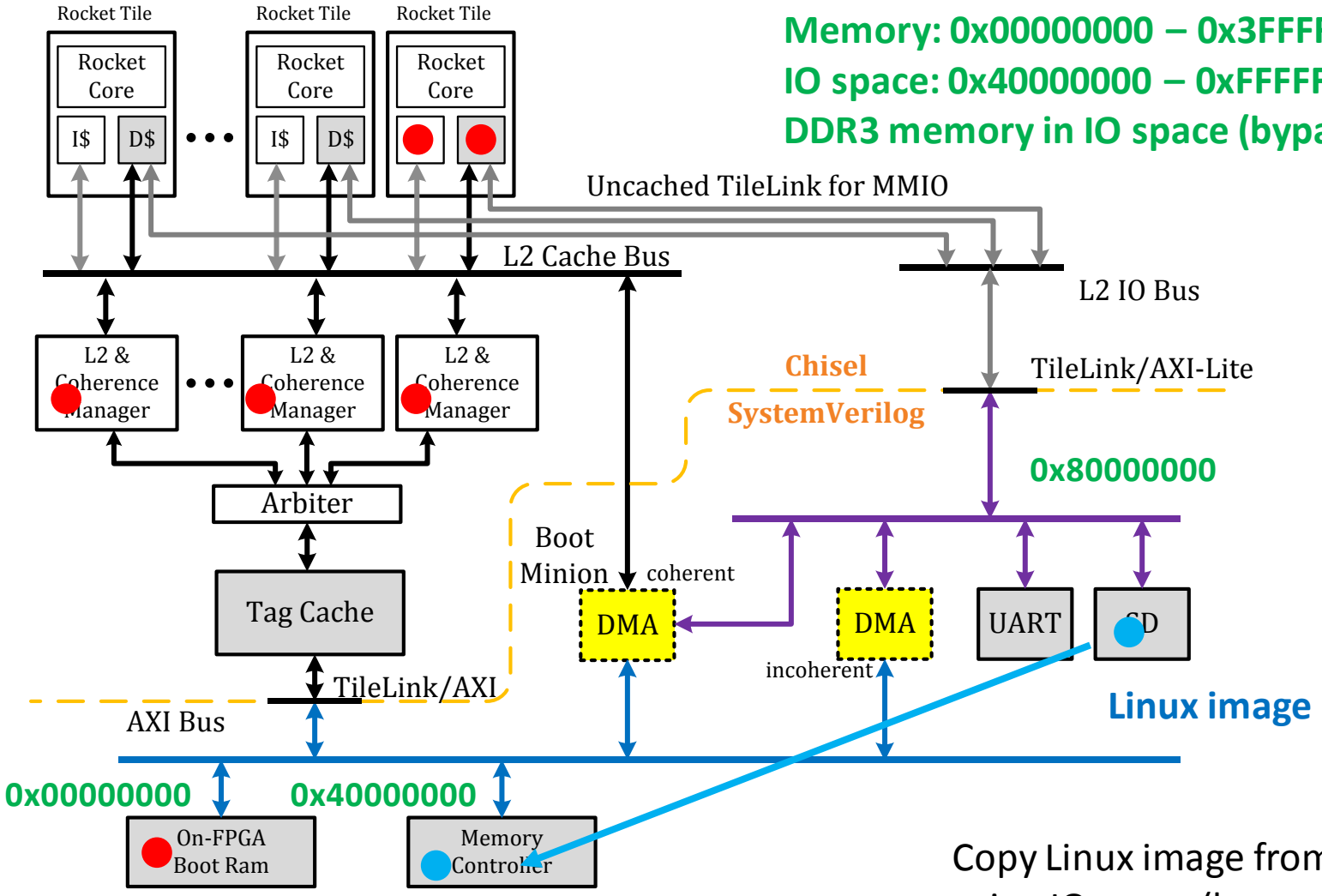
Memory Mapped IO (1)



Memory Mapped IO (2)



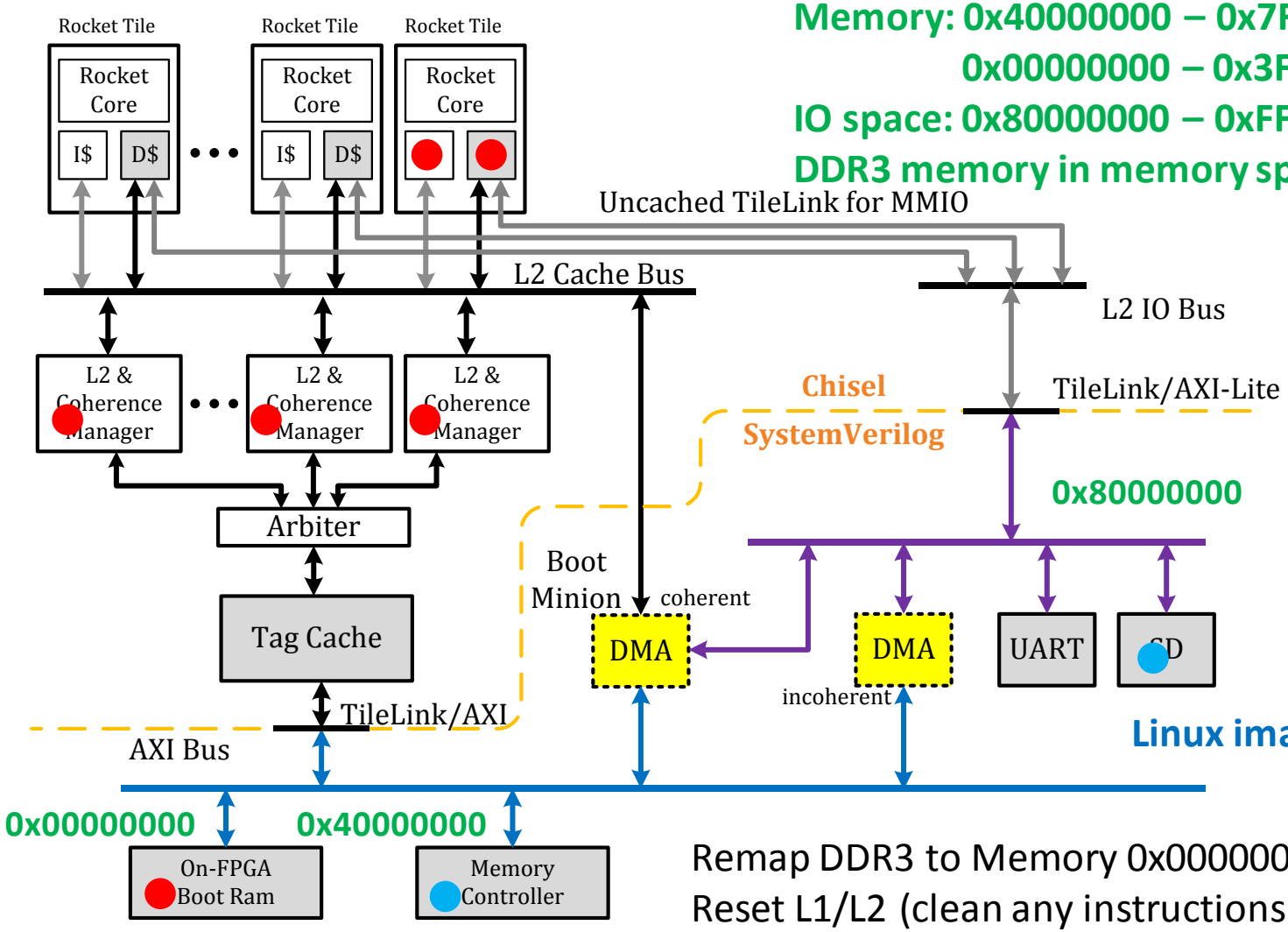
Bootloading Procedure (1)



Memory: 0x00000000 – 0x3FFFFFFF
IO space: 0x40000000 – 0xFFFFFFFF
DDR3 memory in IO space (bypass L1/L2)

Copy Linux image from SD to DDR3 using IO space (bypassing L1/L2).

Bootloading Procedure (2)



Memory: 0x40000000 – 0x7FFFFFFF ->
0x00000000 – 0x3FFFFFFF
IO space: 0x80000000 – 0xFFFFFFFF
DDR3 memory in memory space

Remap DDR3 to Memory 0x00000000 – 0x3FFFFFFF
Reset L1/L2 (clean any instructions from bootlaoder)
All must be coded in one cache line (16 insns)

Bootloading Procedure (3)