MANCHESTER 1824

The University of Manchester

GAELS Project Progress

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19/04/2012

Current Status

- Verilog Parser
  - Designing a Verilog parser which can parse synchronous RTL designs.
  - Now support:
    - Able to read in all synthesisable features (except functions)
  - Ongoing
    - Syntax checking, elaboration and design linking

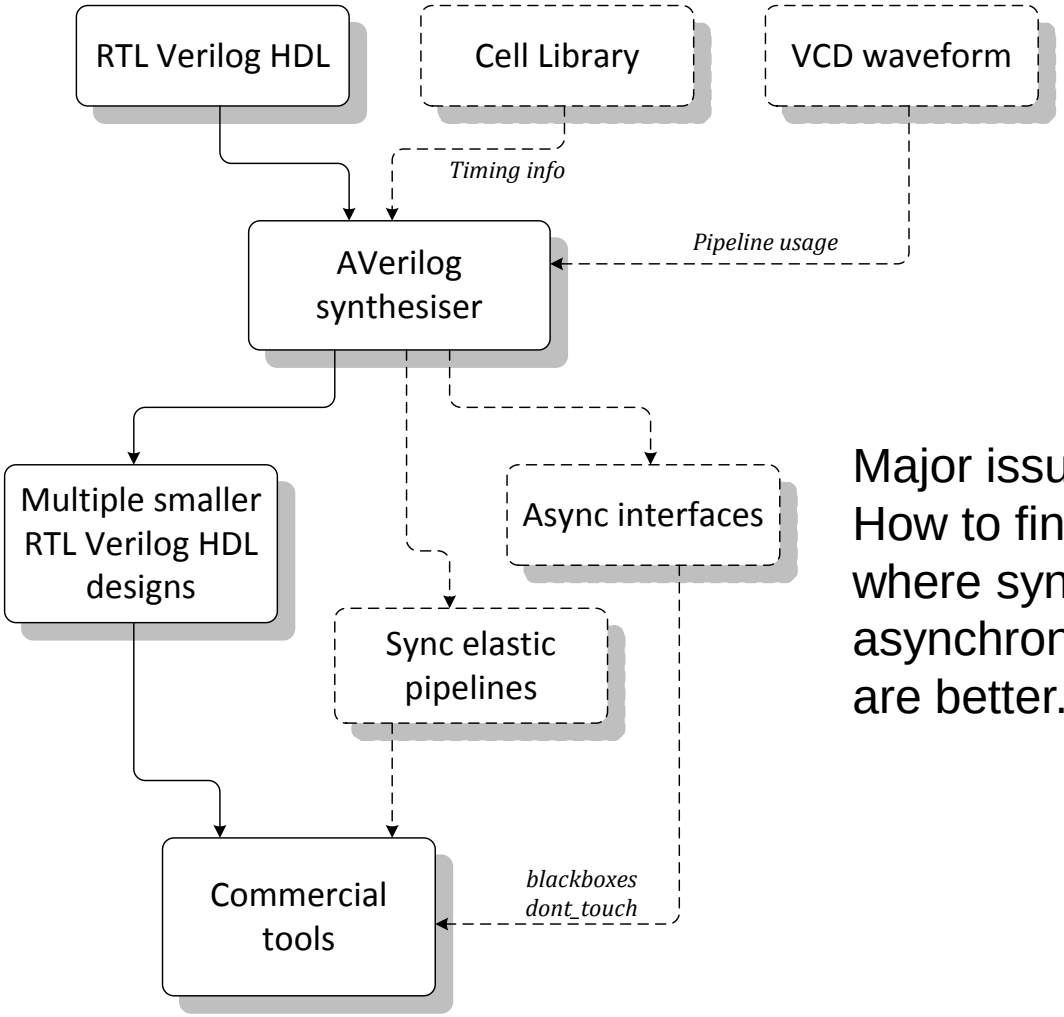
What's next

- Circuit analyses
  - Data-flow analyses
  - Find the optimal boundary for sync/async partition
    - How to find?
  - Convert some part to sync/async elastic circuits.
    - Is sync elastic circuit able to seamlessly connect with sync circuits?
    - How to find the right sub-circuits to be converted?

Parser structure

- Scanner
  - Flexer (lex)
- Lex analyser
  - Bison (yacc)
- Data structures
  - C++0x, STL, boost, GNU MPL
- Remain unknowns
  - Database format, preprocessor

Tool flow



Major issue:
How to find the sub-circuits where synchronous elastic or asynchronous implementations are better.